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TECHNOLOGY APPLICATIONS
FOR TACTICAL DATA SYSTEMS

FINAL REPORT
30 DECEMBER 1966

prepared for

Naval Analysis Staff
Naval Research Laboratory
Washington, D.C.

under
Office of Naval Research (462)
Contract Nonr-4910(00)

by

Hobbs Associates, Inc.

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PREFACE

This report presents results of the Hobbs Associates
analysis and evaluation of trends in application of
advanced data processing technology for future Naval
tactical data systems. This task, sponsored by the
Office of Naval Research and Ships Systems Command,
was carried out as a part of the Naval Command System
Research Program of the Naval Research Laboratory
directed by Mr. Ralph G. Tuttle, Scientific Officer.
The objective of this program is to provide a scientific
and technological base on which system planners can
make improved decisions in the development, design,
and implementation of improvements to Naval Command
and Control Systems.

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1 1 INTRODUCTION

This report presents the results of a study of Technology Applications
for Tactical Data Systems.   The purpose of the study is to provide the
necessary technical information and evaluations of new technologies to
permit systems planners to make proper decisions concerning the se-
lection of hardware for implementing any necessary functions in 1970 to
1980 era tactical data systems.   This study is intended to provide guidance
for Navy systems planners both in the selection of hardware to meet per-
formance requirements and in the proper utilization of new technologies
to implement systems requirements and improve maintainability of future
data systems operating in a tactical environment.

This report covers the three major phases of the study.   The first in-
volved the study and evaluation of new hardware technologies that will
be used by systems planners in planning Navy and Marine tactical data
systems for the 1970 to 1980 era.   The study of hardware technology,
which includes component and packaging techniques, memories, displays,
and input/output equipment, is closely related to the Marine Tactical
Command and Control Study (MTACCS) and the Advanced Naval Tactical
Command and Control Study (ANTACCS), Phase I and Phase II, by
Informatics, Inc   System requirements and information on hardware
capabilities have been exchanged by Informatics and Hobbs Associates
during these studies.   A second phase dealt with the implications of
new hardware technologies to systems design and Naval applications.
A third phase dealt with the effect of new technologies on the maintain-
ability of future tactical data systems, ways in which maintainability
considerations will influence the utilization of new technologies, and
changes in maintenance concepts necessary to properly utilize new
technologies to improve maintainability.

The manner and extent to which technical information is presented is influenced by the fact that part of this study is a follow-on to a previous study of hardware technology conducted in conjunction with Informatics as part of the ANTACCS study. The results of the previous investigations and evaluations of hardware technology are presented in great detail in Volume V of the ANTACCS Final Report. This is particularly true with respect to components and packaging techniques, memories, large screen displays, and conventional input/output equipment. Hence, in these areas this study has concentrated on the investigation and evaluation of newer research and development efforts and on monitoring, validating, and updating the status and expectations for the more important technologies that were covered in the ANTACCS Final Report. Emphasis has been placed in this study on the relationship of new technologies and packaging techniques to systems design and maintainability.

1.2 TECHNOLOGY ADVANCES

The progress in electronic and magnetic batch-fabrication technologies, which has been much more rapid than had been anticipated by most of the industry, promises significant improvements in size, weight, power, cost, and failure rates. The term "batch-fabrication" refers to processes that provide the ability to fabricate simultaneously, in a single set of processing operations, large numbers of circuit elements and the interconnections necessary to connect them into circuits. Batch-fabrication techniques permit not only the fabrication and interconnection of the elements of an individual circuit, but also of large arrays of circuits with the appropriate interconnections between circuits to form a major function or group of functions.

Feasibility has already been proven for many new technologies and several of them have been utilized in production equipment. However, the products available today employing these new technologies represent only the initial

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steps in a revolutionary change in electronic and magnetic equipments. For example, a single monolithic integrated circuit mounted in a flat pack, which represents a major advance over the equivalent circuit fabricated from discrete components on a printed circuit board a year or two ago, will be replaced within the next few years by large inter-connected multi-circuit arrays fabricated on a silicon chip. Each such chip may contain hundreds or thousands of interconnected circuits. Several multi-circuit arrays of this type can be interconnected by vacuum deposited wiring patterns on substrates and packaged as a single large unit. The use of large arrays of circuits which permit most of the interconnections to be made by batch-fabrication techniques and which permit amortizing packaging and external interconnection costs over a large number of circuits in the package will be essential to achieve the true low cost potential of integrated circuits.

By 1970 logical circuits will be available in large interconnected circuit arrays costing 3 to 5¢ per circuit and capable of providing speeds in the order of .5 to 10 nanoseconds propagation delays and 10 to 50 megacycle clock rates. Main internal memories will be available costing between 1 to 3¢ per bit and providing read/write cycle times in the order of 0.3 to 1 microsecond with capacities in the order of 100,000 words. High speed control or scratch-pad memories are expected to cost from 2 to 5¢ per bit and solid-state random access on-line auxiliary storage from 0.2 to 1¢ per bit. Failure rates for digital circuits in the order of .0005% to .0001% per thousand hours are anticipated for the early 1970's.

Large-screen dynamic displays that do not depend upon electromechanical, photographic, or optical projection systems will be feasible along with flat-panel console type displays that are completely compatible with batch-fabricated solid-state electronics. New types of input/output equipment and solid-state replacements for some conventional types of

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input/output equipment will be feasible, but input/output equipment and large capacity mass memories will represent the major problem areas in future tactical systems with respect to size, weight, cost, reliability, and maintainability.

1.3 SYSTEM IMPLICATIONS

Batch-fabrication technologies providing significantly lower central processor hardware costs will create serious system imbalances. If large-scale integrated circuit arrays and batch-fabricated memories are effectively utilized, the dominant factors in systems cost will be software and electromechanical input/output and mass storage devices. Designers of future computer systems will face three major problems:

1. The necessity of developing machine organization techniques that permit the efficient utilization of large arrays to achieve their true potential in cost, reliability, and maintainability.

2. An urgent need to develop new and improved types and minimize the amount of electromechanical mass storage and input/output devices to reduce systems cost and increase systems reliability.

3. An equally urgent need to minimize the cost of providing systems software - both operating systems and user programs - even if this significantly increases the central processor hardware.

Large scale integrated circuit arrays and other batch-fabrication techniques will make it possible to fabricate and interconnect major portions of a computer in a single replaceable unit, but logic design and machine organization techniques must be developed to permit computers to be organized in

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large functional blocks to a much greater extent than at present. This will be necessary in order to minimize the interconnections between functional blocks and the number of leads that must be brought out from each functional unit. Several possible approaches to this should be considered including parallel processors and modular multi-computer systems.

The solid-state electronic and magnetic portions of large digital systems are more amenable to batch-fabrication. Hence, central processors, internal memories, and solid-state auxiliary memories will benefit to the greatest extent from new batch-fabrication technologies. The digital logic, control, and storage functions in displays and input/output equipments will also benefit from batch-fabrication technologies since they utilize similar components and circuits. However, only limited improvements will be achieved in the portions of displays, very large capacity auxiliary storage, and input/output equipments that require high voltage circuits, high-powered circuits, electro-mechanical components, or optical projection devices. These will continue to present major problems with respect to cost, size, weight, maintainability, and reliability. Hence, a serious system imbalance will result unless solid-state electronic or magnetic replacements are developed for present types of displays (visual transducers), mass memories, and input/output equipments.

The best approach to overcoming input/output problems seems to lie in developing system techniques that minimize the need for this type of equipment. A major step in the direction is the greater utilization of on-line systems concepts including capturing data at its source and providing consoles for direct man-machine interaction. Unless extensive additional research and development efforts are initiated in input/output equipment and large capacity mass memories, these devices will be the limiting hardware factors in the capability and performance of future systems.

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Software and programming costs now represent at least 50% of the initial cost of a new computer system a id perhaps as much as 80% of total systems operational costs over a ten year period. The rapid reductions in hardware cost resulting from new batch-fabrication technologies will magnify this software problem. Software costs will be a major limiting factor in future systems unless machine organization and system design concepts are changed to utilize more low cost hardware to implement many functions presently handled by software and to simplify the programming function.

Low cost logic and storage will greatly increase the capability of computers and will make possible the use of special purpose computers in applications that have not been practical heretofore. For example, equipments such as displays, radars, sonars, etc. may contain their own special purpose computers which operate on-line with a large central computer exchanging data and work as necessary.

1.4 MAINTAINABILITY

The efficient utilization of batch-fabrication technologies will require a significant increase in the functional size and complexity of replaceable or throw-away units. Hence, although the cost per component or per circuit will be only a fraction of present costs and the number of packages will be greatly reduced, the batch-fabrication and interconnection of large arrays of circuits in a single package may cause an increase in the total cost of an individual package. It has become apparent that functionally large throw-away units not only are desirable from the standpoint of batch-fabrication technologies but also provide a key to significant improvements in maintainability. The use of throw-away units that are significantly larger from the standpoint of function and complexity will be permitted by the lower cost per component and the lower failure rate afforded by batch-fabrication technologies.

If maximum advantage is to be taken of the capabilities of batch-fabrication for small size, low cost, and high reliability, it will not be feasible to make repairs in a packaged unit on shipboard, and probably not at a stateside repair depot. Hence, to realize the full potential of batch-fabrication techniques it will be necessary to increase the functional size, complexity, and cost limits presently established for throw-away units. Any increase in the cost of the unit will be offset to a large extent by the increased reliability and hence lower failure rates.

Increasing the functional size and complexity of the throw-away unit will improve maintainability by:

Reducing training and skill levels required by maintenance personnel,

Reducing the number of maintenance technicians required,

Reducing supply and logistics requirements,

Simplifying and speeding fault isolation,

Minimizing down time.

These improvements will both reduce maintenance costs and increase systems availability.

If the complete central processor is packaged in a total of 10 or 15 packages, maintenance will consist of locating the fault in one out of 10 or 15 units and replacing that unit. Fault location can be accomplished primarily by diagnostic programs with consequent reductions in maintenance, personnel and skills. With significantly higher MTBF's, even this type of maintenance will be required very infrequently. It is reasonable to expect that some time during the 1970 to 1980 period a complete central processor will become a replaceable unit. If a multi-computer system concept based on the use of identical small modular computers is adopted, such small modular computers may even become throw-away units in the 1975 to 1985 period.

Future maintenance concepts should be based on the use of very large functional throw-away units and on no shipboard repair for electronic portions of the data handling system. Shipboard maintenance will be required for the electro-mechanical equipment that cannot be eliminated from the system. Adopting this approach to maintenance will require significant changes in concepts and attitudes towards maintenance on the part of Navy systems planners, budgeters, and users.

1.5 IMPACT ON FUTURE NAVAL SYSTEMS

The impact of new technologies on naval tactical systems by the early 1970's will be profound. The impact of these new technologies will be reflected not only in lower cost and increased performance capability, but also in reduced size and weight and increased reliability and maintainability. Even if no performance or application requirements exist for the development of new systems, the significant improvements that new technologies will make possible in size, weight, reliability, and maintainability will justify the development of a new generation of tactical data systems.

In the early 1970's, a batch-fabricated computer with capability equivalent to that of the present USQ20B will cost in the order of $25,000 compared to approximately $125,000 for the most recent USQ20B procurement. Such a computer can be packaged in ten or fifteen replaceable units each costing in the order of $1,500 to $3,000. Anticipated reliability improvements between one and two orders of magnitude will result in mean-time-between-failures in excess of one year for a complete computer. Hence, it will be reasonable to consider each of these ten or fifteen packages as a throw-away unit. This will reduce computer maintenance to merely locating the fault in one of ten or fifteen units, which can be achieved by a relatively simple diagnostic program, and then replacing that unit. Later during the 1970-80 period, the complete computer will become a replaceable unit and possibly a throw-away unit in the 1975-80 period.

Flat panel displays will significantly reduce the size of consoles and the space required for operator and command functions requiring display consoles. The console size resulting from the use of flat panel displays will also permit the use of remote consoles in locations where space has been too limited. The compatibility of some flat panel display techniques with integrated circuit current and voltage levels will further reduce console size and power requirements and increase reliability. Large-screen displays will be available for group operations and command briefing and decision making.

Reductions in the order of 25.1 in the size and weight of certain parts of tactical data systems, such as the central processor, are anticipated. For the over-all data handling and display portions of typical NTDS installations, new technologies feasible for use in 1970 will permit reductions of approximately 2/3 in the size, weight and power requirements. Implications of these reductions, particularly for small ships, are clear. The accompanying reductions in system down time and maintenance personnel make it imperative that the Navy plan to take advantage of these new hardware technologies at the earliest possible time.

1.6 CONCLUSIONS AND RECOMMENDATIONS

The major problem areas for tactical data systems in the 1970 era will be:

Input/output equipment

Very large capacity auxiliary storage

Large-screen displays

Machine organization and system design concepts to effectively utilize batch-fabrication technologies.

Concepts and philosophies for maintenance of batch-fabricated equipment.

Software

The impact of new technologies on naval tactical systems will be profound. The use of these new technologies will provide:

Lower costs

Increased performance and capability

Greater flexibility and usefulness

Closer man-machine interaction

Reduced size, weight, and power

Increased reliability and maintainability

The improvements that are expected in size, weight, and power requirements are illustrated by comparing present NTDS equipments with estimates for equivalent equipments that will be achievable in 1970. These comparisons indicate a 25-1 reduction in the size and weight of a central processor and a 3-1 reduction in the size, weight

and power requirements of the overall data handling and display portions of the system.

It is not necessary to wait for the development of a complete new system to achieve some of these advantages. Some of them can be achieved within the next few years in an evolutionary manner by replacing individual equipments.

System requirement studies and analyses for future data systems in the Navy will undoubtedly indicate increased performance require- ments and new applications for future systems. However, even if no performance or application requirements existed for the develop- ment of a new system, the significant improvements that new tech- nologies will make possible in size, weight, reliability, and main- tainability will justify the development of a new generation of tactical data systems.

Specific recommendations concerning each of the 4 hardware tech- nology areas covered by the study are presented in Section 2 follow- ing the discussion of each technology area. In addition to those detailed recommendations on specific technologies, several broader recommendations of greater overall importance to Navy systems planners are presented below:

   1. Batch-fabrication technologies, including large-scale integrated circuit arrays and batch-fabricated magnetic memories, offer such significant advantages over pre- sent discrete component technologies that Navy systems planners should utilize them at the earliest possible

time. Navy R & D activities should also support the further development of these technologies where necessary support is lacking from other sources.

2. Future equipments and systems should be designed to maximize the advantages offered by batch-fabrication technologies, particularly with respect to the utilization of large functional modules that maximize the number of circuits within a module and minimize the number of external leads and connections required between modules.

3. Block-oriented-random-access-memories (BORAM) and other approaches to solid-state on-line auxiliary storage should be developed and utilized to provide a larger amount of on-line storage for the system and to minimize the requirements for electromechanical auxiliary storage and input/output equipments.

4. Flat-panel displays should be developed and utilized for both large-screen and console applications in order to provide a satisfactory large-screen display and to significantly reduce the physical size of console displays. The visual transducer in such flat-panel displays should be amenable to batch-fabrication and compatible with batch-fabricated electronic and magnetic components.

5. Development of new types of input/output equipment that utilize solid-state electronic and magnetic technologies rather than electromechanical techniques should be supported.

6. System organization concepts and techniques for future systems should emphasize on-line operation to the greatest extent possible to minimize the need for conventional types of input/output equipment.

7. Research in new machine organization (system architecture) techniques to permit more highly functional and modular organizations should be supported so that a computer can be assembled from a limited number of large functional blocks to facilitate utilization of large batch-fabricated arrays. Such investigations should include repetitive use of functional arrays within a large computer, small standard modular computers for multi-computer systems, parallel processing systems, and other types of "non-conventional" machine organization concepts.

8. Future systems should reflect different trade-offs between hardware and software because of the availability of low-cost logic and storage hardware

and increasing software costs. Such altered hardware/software trade-offs may include special purpose computers and processors, new machine languages and organizations, new programming languages, and hardware implementation of functions presently implemented in software. Research in these areas and utilization of such techniques in future systems should be encouraged and supported.

9. Navy systems planners should insist that systems designers and contractors consider large-scale integrated circuit arrays as a new type of device that necessitates major revisions in systems design concepts, machine organization, and hardware/software trade-offs.

10. Future maintenance concepts should be based on the use of large functional throw-away units leading eventually to the elimination of shipboard and field repairs within functional modules. Shipboard and field repairs should be reduced to fault location by diagnostic programs, replacement of large functional modules, and discard of faulty modules. The replacement cost of large and relatively expensive throw-away modules can be justified by significantly decreased failure rates and reductions in maintenance personnel.

11. A new generation of tactical data systems should be developed to take advantage of the significant improvements that new technologies will make possible in size, weight, reliability, and maintainability in addition to any performance or applications requirements that may exist for the development of new systems.

2. OVERVIEW OF ADVANCED HARDWARE TECHNOLOGIES

Subsequent sections of this report discuss the implications of advanced hardware technologies on computers and digital systems, maintainability, and future naval tactical systems. To provide a basis for considering these aspects of future systems, this section provides an overview of advanced technologies by summarizing the major aspects of each of the categories of hardware technology investigated during the study. Each of the four major categories - components and packaging, memories, displays, and input/output - are discussed in greater detail in Appendices A, B, C, and D respectively.

This section serves as a summary of each of those four appendices. The major characteristics of the more promising advanced technologies are summarized and problems or advantages in their utilization in future systems are highlighted. Since each of these four categories of hardware technology were covered in detail in Volume 5 of the first ANTACCS report, particular attention is given to any new technologies and to changes in the status or feasibility of technologies covered in the ANTACCS report. While major recommendations concerning the impact and utilization of advanced technologies are presented in Section 1 of this report, more detailed recommendations concerning each of the four areas of technology are presented in this section.

This study was concerned only with technologies useful for future naval tactical systems; hence, it was necessary to establish criteria for selecting the technologies to be investigated during the study that would best utilize the available time for this purpose. These criteria are described in this section.

2.1 CRITERIA FOR SELECTING TECHNOLOGIES TO BE INVESTIGATED

Potential uses and advantages in future naval tactical systems were the major criteria used in selecting technologies to be investigated in this study. Investigation was not considered justified merely because a technology is interesting or different. It must fill some need or offer some potential advantage to Navy systems planners for future tactical data systems.

The needs of the systems planner are influenced by both system requirements and systems design. The systems requirements determine functions that must be implemented, and the systems design determines the way in which these functions are implemented. Both affect the usefulness of a particular technology. Conversely, the characteristics of one type of technology compared to those of another type can influence the way in which the function is implemented. In fact, the availability of a new technology at a low cost and high reliability can make it feasible to implement functions that were not previously justifiable on a cost-effectiveness basis, thus changing the analysis of systems requirements.

After a requirements analysis and systems design based on those requirements have been completed, it is relatively easy to limit the scope of an investigation of technologies for implementing the system. However, requirements analysis and preliminary systems design for future Navy and Marine Corps tactical systems were underway concurrently with this study of hardware technologies. Hence, a good deal of judgment was necessary in determining which technologies should be investigated. It was considered better to investigate a technology that may not be used than to overlook one that might offer significant advantages to planners of future systems, but it was necessary to limit the number of technologies to be investigated in order to concentrate on those that offer the greatest potential for future tactical data systems. In order to accomplish this,

four specific criteria were applied in selecting technologies for investigation:

1. Is the technology useful for implementing functions existing in the present Naval Tactical Data System or Marine Tactical Data System?

2. Is there some known Navy or Marine Corps operational task for which the technology offers potential advantages, even though the task may not presently be mechanized or may be implemented in a completely different manner?

3. Does the technology represent a sufficiently significant advance in the state-of-the-art that systems planners will find a worthwhile use for the technology even though no requirement is known at present?

4. Does the technology offer important potential advantages over existing alternative technologies without suffering from any decided or overriding disadvantages within the context of a tactical operating environment?

Is the technology useful for implementing functions existing in the present NTDS or MTDS?

Since the present operational systems have been designed on the basis of earlier analyses of requirements for tactical data systems, future systems will probably require the same types of hardware functions, although alternative technologies may be used where they offer advantages. For example, console displays are an integral part of the present NTDS system; hence, it is very likely that technologies for implementing console displays will be required in future tactical data systems. This type of justification also implies the need for most types of components and devices used in conventional computer systems. For example, implementing a

computer or data processing system in accordance with known and foreseeable computer design concepts requires logical circuitry and internal storage.

The four major categories of technologies to be investigated - components and packaging techniques, memories, displays, and input/output - were selected on this basis. This also served as the first criteria in selecting specific technologies to be investigated in each of these categories including:

      Components and packaging techniques

           Logical circuits for implementing logic in the central

                  processor and in peripheral equipment

           Linear circuits (e. g. memory sense amplifiers)

           Interconnection techniques

           Packaging techniques

      Memories

           Registers and high-speed control memories

           Main internal memories

           On-line auxiliary storage

           Off-line auxiliary storage

      Displays

           Console displays

      Input/output equipment

           High speed block serial input

           Low speed incremental serial input

           Keyboard input

           Character printers

Is there some known Navy or Marine Corps operational task for which the new technology offers potential advantages?

Some technologies not used in the present NTDS or MTDS may offer advantages in implementing specific functions in future tactical systems.

Requirements for specific hardware capabilities and requirements for
implementing specific functions developed by Informatics in Phase I
and Phase II of the ANTACCS study and in the MTACCS study provided
the basis for most of the criteria in this category. If functions or tasks
in Navy and Marine Corps tactical systems can be identified for which a
technology offers potential advantages, this was considered sufficient
justification for investigation of that technology. Systems planners may
or may not decide to use the technology in a future tactical data system,
but the technology must be evaluated in order to provide technical informa-
tion the system planner will need in order to make that decision.

For example, associative memories that permit addressing stored informa-
tion by content rather than by physical location offer some advantages in
track while scan and threat evaluation and weapon assignment operations.
A system planner must have information about associative memories in
order to decide whether those advantages justify the cost of an associative
memory in contrast to alternate approaches such as programming a memory
search in a conventional high-speed random access memory.

Hence, if a use for a technology could be identified in which it offers
potential advantages to a systems planner, that technology was investi-
gated in this study.

Thus, the systems planner will have the necessary information to properly
evaluate the use of alternate approaches in the design of a future system.
Examples of such technologies and brief reasons for including them in
the investigations in this study are:

> Associative memories - potentially useful in several functional
> tasks including track while scan and threat evaluation and
> weapon assignment.

Read-only memories - potentially useful for microprogrammed (stored logic) machine organizations, fixed program storage, and storage of data that is changed relatively infrequently (e. g. screen patterns in multi-ship ASW operations).

Large screen displays - potentially useful for Flag presentations and CIC plots.

Character recognition equipment - potentially useful for reading data initially entering the system in printed form.

Voice recognition and voice output equipment - potentially useful for direct communication with the computer without the need for manual operations such as keypunching.

Graphic input equipment - potentially useful for directly entering graphical information such as flight paths and formation and maneuver patterns.

The selection of technologies in this category assumes that the role of future tactical systems will expand beyond that of anti-air operations (the major function of the present NTDS and MTDS systems), envisions the possibility of closer integration of tactical data systems with weapons systems and sensor systems in the future, and envisions the inclusion of functions such as intelligence data processing. Only by understanding the full range of technologies available can a systems planner adequately determine the capabilities that can be implemented in a future tactical system and the alternative methods of accomplishing this.

Does the technology represent a significant advance in the state-of-the-art that will cause it to be used for functions not presently anticipated? Some new technologies may be developed that advance the state of the computer art in a major way. If this occurs, it is very likely that designers of future systems will see ways of utilizing the new technology to achieve results that are not possible with present kinds of equipment. If such technologies appear, they should be investigated whether a specific requirement can be foreseen or not. However, no technologies in this category were discovered during the study.

Does the technology offer important potential advantages over existing alternative technologies without suffering from any decided or overriding disadvantages within the context of a tactical operating environment? This criteria was superimposed on the first three. Regardless of whether a use exists or is anticipated for a new technology, there is no point in considering it unless there is reason to believe that it may be better than existing well established technologies. For example, evaluating a new storage technology would be a waste of time unless it has some potential advantages over magnetic core memories.

Many technologies were eliminated from consideration in this study because they did not offer sufficient advantages over better established approaches. Hence, a good deal of judgment has been exercised in limiting the study to those technologies that are useful, applicable to tactical environments, and worthwhile. No attempt has been made to evaluate in detail every different technique or approach.

2.2 COMPONENTS AND PACKAGING

For the past five to seven years discrete component semiconductor circuits have dominated the computer data processing field as logic components. A number of alternatives to transistor and diode electronic

circuitry have been proposed but none of these have proven superior for the majority of applications. These alternatives include cryogenic logic, fluid logic, all magnetic logic, and optical logic. Cryogenic and optical logic are yet to be proven feasible. Fluid and magnetic logic offer some advantages in slow speed applications, such as the implementation of control functions in input/output equipment, and in some adverse environments. However, semiconductor integrated circuits, which are rapidly replacing discrete component circuits, will be dominant for the foreseeable future - probably for the next ten to fifteen years at least.

Present integrated circuits with limited numbers of components or gates per chip will give way to a large extent within a few years to large scale integration. Large scale integration or LSI is a term commonly used to designate large arrays of integrated circuits with hundreds or thousands of gates or other circuits interconnected on a single silicon chip. LSI will play a major role in the dramatic changes in computer systems design and applications that will occur within the next few years.

Closely related to basic integrated circuit technology are the associated technologies for batch fabrication of interconnections. The two major techniques are vacuum deposition of metallic interconnect patterns through masks and printing of metallic interconnect patterns by processes similar to silk screening in the graphic arts. Batch fabrication is the key to low cost high reliability components and interconnections for both logical circuitry and internal memories. Major improvements in cost and reliability can be achieved by fabricating large arrays of circuits on a single silicon chip and interconnecting these on the chip. In order to minimize the number of interconnections brought from the chip it will be necessary to develop logical design and machine organization

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techniques that facilitate the organization of the machine into large functional units with a minimum number of interconnections required between these functional units. For example, either an adder or perhaps an entire arithmetic unit may be fabricated on a single large chip with external connections required only for input/output and control signals. Another approach is to fabricate the unit on several large chips which are then interconnected by wiring deposited on a substrate and packaged as a single unit. This is directly related to the subject of throw-away unit size and maintainability discussed in Section 4.

Particular attention was given during this study to those component technologies for 1970 era systems that appeared most promising during the 1964 ANTACCS study including:

> Monolithic integrated circuits
> Hybrid monolithic/thin-film integrated circuits
> Active thin-film integrated circuits
> MOS integrated circuits

Consideration was also given to other component technologies whose feasibility or applicability appeared questionable during 1964 including:

> Optical logic
> All magnetic logic
> Fluid logic

However, subsequent developments have not indicated any significant changes in the applicability of these approaches.

The following levels of packaging and specific packaging techniques were investigated:

> Multi-circuit chips
> Cellular logic

Multi-function logic

Variable interconnections

Fixed interconnections

Multi-chip substrates

Mother board and back board techniques

Printed circuit boards

Multi-layer printed circuit boards

Multi-layer deposited (or printed) wiring

Connectors

Bonding techniques were also investigated including:

Flip-chips

Welding

Soldering

These technologies were investigated by discussions with technical
experts working in these fields, by studying the applicable literature,
and by evaluating information concerning the different technologies
in relation to the requirements that will be imposed by future naval
tactical systems. This portion of the study was closely related to the
part of the study dealing with the effect of new technologies on main-
tainability. In the evaluation of new technologies, the effect on relia-
bility and maintainability was given major weight. The implications
of large scale integration (LSI) to maintainability are discussed in
Section 4 of this report.

2.2.1 Technical Summary

The investigations during this study confirmed and supported the major
evaluations, conclusions, and recommendations made during the ANTACCS
study in 1964. However, technological advances in batch-fabrication
techniques since that time have accelerated the rate at which these

techniques will affect Naval systems. The belief that future computers will utilize large arrays of interconnected logical circuits performing major logical functions was confirmed by discussions with semiconductor specialists and by published information. Although there was some controversy about this during the preceding study, the major questions now are when this will be feasible (rather than if) and how large the arrays will be. Many technical experts were optimistically predicting these large interconnected arrays in 1964, but now even the managements of major semiconductor companies are publicly announcing that these will be available. For example, Dr. Robert N. Noyce, Group Vice President of Fairchild Camera and Instrument Corporation, addressing the San Diego Council of WEMA stated,

> "However, from a point on the complexity scale now where 50 components in the cheapest level for an integrated circuit, I expect to move to 1000 by 1970.... At the same time there will be new problems where it takes only 10 chips to make a computer and almost every circuit made will be different."

The major controversy now is whether these large arrays will be fabricated primarily with monolithic silicon circuits (using bipolar transistors) or with metal-oxide-semiconductors (MOS). One interesting development since the investigation in 1964 has been the rapid progress of MOS devices. Some in the semiconductor industry believe MOS technology will prove dominant where large arrays are required because of the somewhat simpler processing required. The smaller number of processing steps tends to make more feasible the high yield necessary for large arrays. In monolithic circuits it is necessary to control the thickness of the diffusion layer in the semiconductor, while in the MOS it is necessary to control the thickness of the oxide layer. Hence, the problem of process control is transferred from the body of the semiconductor to the surface. Many feel that surface effects will be a more difficult factor to control,

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but significant progress has been made in this direction. Even if the large MOS arrays do prove easier to fabricate and hence cheaper, they will still suffer from one major disadvantage - speed. The MOS is a field-effect type device with more limited speed capability. Although progress in both technologies is expected, it appears likely that MOS devices will remain approximately one order of magnitude slower than monolithic integrated circuits. MOS devices may be utilized in applications where high speed is not required and in applications where very large standardized arrays can be used. Examples of the latter category are large integrated circuit storage arrays for main internal memory. Monolithic integrated circuit storage arrays will be faster, but slower speed MOS devices may be sufficiently cheaper to make their use in larger capacity memories more feasible.

It is believed that monolithic integrated circuits will be the dominant technology for high speed control (scratchpad) memories and logic circuits in the type of computers of interest for future tactical data systems. Hybrid monolithic/thin-film circuits may be used for linear amplifiers where high values or high tolerance resistors and capacitors are required. Examples of circuits of this type are memory sense amplifiers and video amplifiers in displays. The use of additional active elements in the monolithic circuit can permit compensation in some cases where high value or high tolerance resistors or capacitors would otherwise be required.

During the 1964 study, considerable interest and speculation was found concerning the eventual role of active thin-film circuits. However, relatively little emphasis on this technology has been found recently. This is believed to be a result both of serious technical problems in active thin-film technology and of the very rapid and significant progress being made in monolithic and MOS integrated circuit technologies. Many of the

advantages anticipated for active thin-film devices can be realized in
the near future with monolithic and MOS technologies. Hence, even if
active thin-film devices prove feasible, their impact will not be felt
in Naval systems until the late 1970's - the 1975 to 1980 period.

In considering large-scale integration (LSI) one is faced with two major
problems:

The possible need for eliminating bad or substandard circuits
from the array to achieve a reasonable yield.

The lack of flexibility resulting from large arrays which tends
to make each array within a system unique.

Three major approaches to the utilization of large interconnected arrays
from the systems standpoint are under consideration. The first is
cellular logic in which large arrays of identical circuits are fabricated
with a standard interconnection pattern (e. g. connecting each circuit
only to its four adjacent neighbors) with the ability to modify the function
of the circuit by changing something in the circuit subsequent to fabrica-
tion. For example, one approach of this type uses a circuit with four
cut-points which can be cut in different combinations to alter the function
of the circuit.

In the second approach, called "discretionary wiring", a large array of
circuits is fabricated and each circuit is individually tested. The test
results are put in a computer which is also storing logical equations of
the function to be implemented. The computer then generates the proper
interconnection pattern to interconnect available good elements (skipping
the bad ones) to perform the required logical function. In this approach,
a separate mask must be prepared for each array fabricated; hence,
cheap methods for producing interconnection masks under computer control

are required to make this approach economically feasible. Several such mass fabrication techniques are under development. This approach offers a major advantage in that it is easy to vary the function performed by the array by changing the logical equations supplied to the computer. If each interconnection mask for each array is generated individually, there is little incentive for rigidly standardized functions. This ability to "customize" the circuit array will be an important factor for small volume production of functions that are not used in a highly repetitive manner. However, it is important to distinguish between this advantage of discretionary wiring and the advantage of yield enhancement. The importance of the latter is dependent upon the yield obtainable for a given array complexity at any point in time.

The third approach is advocated by those who believe that in the future it will be technically feasible to achieve high yields of large integrated circuit arrays in which all circuits are good. This will permit a standardized interconnect pattern to be used for each specific logical function. This has the advantage that only one mask need be made for a particular function which can then be used to interconnect the circuits in many arrays of that type. However, flexibility suffers since changing the function to be performed by the interconnected circuit array requires making a different mask. Ultimately discretionary wiring will probably be used to customize circuit arrays for infrequently used functions and small volume production while fixed interconnect masks will be used for standardized functions (e.g. a storage array or perhaps an arithmetic unit) or volume production items.

The major types of integrated circuits presently under development with characteristics anticipated by 1970 and brief comments on the advantages or disadvantages of each are shown in Table 2-1. The speeds shown in Table 2-1 for different types of circuits are chosen to be realistic, but

Technology	Performance Anticipated by 1970	Comments
Hybrid discrete/ thin-film circuits	1 to 10 ns propagation delay 5 to 20 mc clock rate	Useful where high ratio of passive to active components is required (e.g. linear circuits) and where higher power capability is required. Higher cost and probably lower reliability.
Monolithic circuits	0.5 to 10 ns propagation delay 10 to 50 mc clock rate	Low cost, high speed, and high reliability. High value and high tolerance passive components are very difficult, but the use of extra active elements can help compensate for this.
Hybrid monolithic/ thin-film circuits	1 to 10 ns propagation delay 5 to 20 mc clock rate	Compromise between the advantages and disadvantages of discrete components and monolithic circuits. More expensive than monolithic circuits but useful for linear circuits requiring higher tolerance passive components.
Metal-oxide-semiconductor (MOS) circuits	20 to 100 ns propagation delay 2 to 10 mc clock rate	Simpler to make and easier to fabricate large arrays of interconnected circuits. Lower power consumption. Speed approximately one order of magnitude slower than monolithic circuits.
Silicon-on-sapphire circuits	20 to 100 ns propagation delay 2 to 10 mc clock rate	Fabrication suitable for large arrays. Promising, but presently being pushed by only one company.
Active thin-film circuits	Will not be available by 1970	Potentially cheaper and easier to fabricate very large arrays. Feasibility is not proven and utilization is much farther away.

MAJOR TYPES OF INTEGRATED CIRCUITS

Table 2-1

many in the semiconductor industry may consider them overly conservative. Costs are expected to range between 3¢ and 5¢ per circuit for monolithic and 2¢ to 4¢ per circuit for MOS techniques in large interconnected circuit arrays. The cost will be somewhat higher for linear circuits requiring thin-film passive elements and may be somewhat lower for highly repetitive functions, such as storage arrays, using large MOS arrays. These figures are intended to indicate cost potentials that can be realized by semiconductor technology, but they can be achieved only by fabricating large arrays of interconnected circuits in a single package since packaging and interconnections are major factors in the cost of an integrated circuit. Hence, the ability to achieve these costs is dependent upon the computer industry's ability to develop logical design and machine organization techniques permitting and utilizing such large arrays. This raises many difficult and conflicting questions, such as packaging design, maintenance philosophy, flexibility, and functional logic segmentation. Some of these are discussed further in Sections 3 and 4 of this report.

2.2.2 Recommendations

Almost all of the electronic components and interconnections in 1970 era Naval tactical systems should be manufactured by batch-fabrication techniques. Monolithic silicon integrated circuits should be used for all logic functions where speed is important and for other electronic circuits wherever possible. MOS arrays may be used for slower speed logic functions, particularly in peripheral equipments, if subsequent developments in both monolithic and MOS technologies substantiate the belief of many people that MOS techniques will be cheaper for large arrays in volume production. However, it is not certain that this will be the case. Many of the low level linear and analog circuits required can be mechanized with bipolar monolithic circuits, but hybrid monolithic/thin-film techniques may be necessary where high precision or high value resistors and capacitors are required that cannot be achieved with monolithic

techniques alone. The use of some discrete components may still be necessary for high power or high voltage circuits such as some of those found in displays and some electromechanical peripheral equipments.

Interconnection and packaging techniques continue to represent the major problem in the effective utilization of advanced circuit and component technologies. Hence, major research and development emphasis should be placed on interconnection and packaging techniques and on machine organization and system design techniques that minimize interconnections external to the package. One of the major limitations at present on the complexity and circuit density of large integrated circuit arrays is the space required for bringing leads in and out of the array. The effective utilization of very large scale integrated circuit arrays will require highly modular machine organization and fabrication techniques that permit interconnecting large arrays of circuits on a silicon chip in order to minimize the number of external leads required. Minimization of the number of external leads will be a much more important design criteria than the efficient utilization of circuits within the package. Design approaches will be required that achieve a very high ratio of number of circuits within a package to number of leads in and out of the package. The use of larger functional packages will both reduce the cost per component and increase the reliability, but attempts to make the package repairable will tend to defeat both advantages. Hence, such large functional modules should be considered throw-away units from the maintenance standpoint.

The number of circuits or logical functions fabricated and interconnected on a single silicon chip should be the maximum feasible within the state-of-the-art at any given point in time. Larger functions should then be fabricated by interconnecting several such silicon chips by means of a

thin-film interconnection pattern on a substrate within an individual package. Since external leads and interconnections will be required between packages, the number of circuits and interconnections within each package should be maximized and the number of packages minimized. Using a thin-film interconnection pattern on a substrate for interconnecting several arrays within a package also permits the fabrication of thin-film resistors and capacitors (for high precision and high values) on the substrate and a higher degree of standardization or common usage of the arrays themselves. Although most of the packages in a system may be unique, a given integrated circuit array on a chip may be used in several packages or in more than one place within a given package. As integrated circuit and batch-fabrication technologies advance, the maximum feasible array size will increase. Hence, a package of a given logical complexity may require several silicon chips in one generation system and only a single silicon chip in a future generation.

No rigid rules should be established for the use of different types of integrated circuits or batch-fabrication techniques. Systems designers should be permitted the maximum flexibility in choosing the combination of hybrid techniques, thin-film components, monolithic circuits, and MOS arrays that best fit the needs of a particular equipment or system. However, emphasis should be placed on achieving the maximum feasible functional complexity in each package to realize the cost and reliability potential of batch-fabrication techniques and to achieve the maintainability improvements discussed in Section 4 of this report.

In summary, the following recommendations are made concerning component and packaging techniques:

1. Use monolithic silicon integrated circuits for high speed digital logic and storage functions and, wherever possible, for low level linear and analog circuits.

2. Use MOS integrated circuit arrays for slower speed, logic and storage functions if the cost per element proves to be appreciably cheaper in volume production.

3. Use hybrid monolithic/thin-film techniques for linear and analog circuits where requirements for high precision or high value resistors and capacitors exceed the capabilities of monolithic techniques.

4. Use discrete components where necessary for high power or high voltage circuits.

5. Design computers and other digital equipment in a way that maximizes the number of circuits interconnected within a package and minimizes the number of external leads and connections required between packages.

6. Use large functional packages to reduce cost and increase reliability.

7. Fabricate and interconnect as large a circuit array on a single silicon chip as is feasible within the state-of-the-art at any given point in time.

8. Permit the system designer maximum flexibility in choosing an appropriate combination of integrated circuit and hybrid techniques for a particular equipment or system.

9. Place research and development emphasis on interconnection and packaging techniques and system approaches that permit large functional arrays.

10. Large scale monolithic and MOS integrated circuit arrays will dominate the computer and digital equipment field during the early 1970's, but research and development in active thin-film devices should be followed closely by the Navy as a possible successor in the 1975 to 1980 period.

2.3 MEMORIES

Several different techniques for batch-fabricating solid-state electronic or

magnetic storage devices are being developed that will provide improvements in internal storage costs and reliability compatible with those for integrated circuit logical components. Very large capacity auxiliary storage requiring electromechanical devices will continue to be a problem area.

For purposes of analysis and evaluation, storage requirements were divided into four major categories based on their functional use:

> Registers and high-speed control memory
> Main internal memory
> On-line auxiliary storage
> Off-line auxiliary storage

Because of the wide difference in characteristics and cost, it is also helpful to differentiate between solid-state on-line auxiliary storage and electromechanical on-line auxiliary storage. A particular type of storage technology may be useful in more than one of these categories but the trade-offs between capacity, speed, and cost will vary with the category.

As with components, batch-fabrication is the key to low cost high reliability memories. In fact, the integrated circuit techniques discussed in the component and packaging section of this report will be directly applicable to the electronic portions of future memories. Monolithic integrated circuits will be used for the straight digital portions of the memory (e. g. addressing, etc.) and some other portions of the memory where linear circuits are required (e. g. the sense amplifier). Hybrid discrete/thin-film circuits may be used where power requirements are too high to be handled conveniently by monolithic integrated circuits (e. g. drivers). ·

Integrated circuit array memories, either monolithic or MOS, in which integrated circuit elements rather than magnetic elements are used for the storage function have been proven feasible and economic - particularly for high-speed scratchpad or control memories. The memory application will be the first use of very large arrays of interconnected circuits on a single silicon chip.

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In any system configuration for tactical data systems in the 1970-1980 period, requirements <u>will</u> exist for:

  Registers and high-speed control memories

  Main high-speed (random-access) internal memories

  On-line auxiliary storage (large capacity)

  Off-line auxiliary storage

Depending upon system design and system requirements, requirements <u>may</u> also exist for:

  Associative memories

  Read-only memories

    Permanent

    Mechanically alterable

    Electrically alterable

    Read mostly

  High-speed serial memories

In this study emphasis was placed on the memory technologies in the first category above. Those in the second category were also investigated briefly where a possible Naval application has been identified. This was the case for both associative memories and read-only memories. Although possible uses for high-speed serial memories can be hypothesized, no specific Naval application of sufficient importance to justify their consideration has been specified to date. One possible use for high-speed serial memories is in a very small, light weight, portable computer for Marine Corps field use, but no definite requirement has been cited for such memories.

Particular attention was given during this study to those memory technologies for 1970 era systems that appeared most promising during the 1964 ANTACCS study including:

Integrated circuit arrays

MOS arrays

Planar thin-films

Plated wires (cylindrical thin-films)

Magnetic cores

Consideration was also given to other memory technologies whose feasibility or applicability appeared questionable during 1964 where subsequent developments indicated that this status appeared to be changing. This category included:

Permalloy sheet toroid

Laminated ferrite

Cryogenic

Of those, only the etched-permalloy toroid memory looks promising. It is one of the major contenders for large capacity random access "mass" memory applications.

Particular consideration was given to technologies for large capacity low cost memories that may provide solid-state replacements for electromechanical magnetic tape units and disc files. This included the ferroacoustic type storage and other BORAM techniques.

These memory technologies were investigated by discussions with technical experts working in these fields, by studying the applicable literature, and by evaluating information concerning the different technologies in relation to the requirements that will be imposed by future naval tactical systems. The criteria for selecting memory technologies to be investigated are discussed in Section 2.1 of this report. The effect of new technologies on reliability and maintainability was given major weight in their evaluation.

2.3.1 Technical Summary

As in the case of component technology discussed previously, the investigations during the first half of this study have tended to confirm and support the evaluations, conclusions, and recommendations made during the ANTACCS study in 1964. The importance and feasibility of batch-fabricated memory arrays have been emphasized by further discussions with memory specialists and by published information. The importance of developing batch-fabrication techniques for connecting the storage arrays to the associated electronics is appreciated by those working in the field. In fact, the ability to easily connect the storage arrays with the associated electronics is a major factor in the evaluation of particular storage techniques.

One significant development during this study was the relative down grading of expectations for batch-fabricated ferrite memories. It is understood that work on the Flute memory has been discontinued. The laminated ferrite memory (now called the "monolithic ferrite memory") is still being pursued, and it is now commercially available in small capacity arrays. However, there has been little public discussion or published information recently on monolithic ferrite memories for large capacity applications. Emphasis now is placed more on their use in relatively small capacity high-speed applications. Although this is a controversial question with many in the memory field having a different view, it is the belief of this study team that the monolithic ferrite memory and other batch-fabricated ferrite memories will not compete successfully with plated wire and planar thin-film memories in the long run.

Another interesting and very significant development during the study was the increasing emphasis on memories fabricated with semiconductor integrated circuit arrays. This is true both for MOS storage arrays and for monolithic integrated circuit storage arrays. Many of those in the

semiconductor field with whom this has been discussed feel that both will be feasible; however, only a few go so far as to say that either will replace magnetic storage techniques for main internal storage. Most seem to feel that their applicability is limited to relatively small memories of a few thousand words or less, except perhaps in unusual environments such as space applications where power is a major consideration. MOS arrays offer a potential for extremely low power consumption in the quiescent state. In general, monolithic silicon arrays are believed to be more applicable for very high-speed small capacity applications (e. g. high-speed control memories) while MOS arrays are more applicable for larger capacity slower applications (e. g. small main internal memories.)

The cost of magnetic core memories is continuing to decrease as production techniques are improved and automated, and speed is continuing to increase as cores are made smaller and smaller. One core memory announced for a high-speed, large-scale, commercial, scientific computer will have a read/write cycle time of 0. 5 us using a 12 mil o. d. and 7 mil i. d. (or smaller) cores. Hence, improvements in the well established magnetic core technology continue to provide a fast moving target for the newer technologies. Some in the memory field believe that automation of magnetic core production and array fabrication will reduce the cost of core memories below the cost that will be achieved by batch-fabricated memories. However, it is the belief of this study team that these production improvements will perhaps extend the time during which the core memory will remain dominant but that batch-fabricated memories will inevitably replace discrete core memories at some point in the future. It is further the belief of this study team that this point will occur by the early 1970's.

Plated wire memories are still considered the most promising with planar thin-film and integrated circuit arrays following closely.

There is a strong likelihood that integrated circuit arrays will quickly
dominate the register and high-speed control memory area. Both pla.ed
wire and etched-permalloy-toroid memories appear promising for large
capacity random access 'mass' memory applications.

The characteristics anticipated for solid-state storage devices in 1970
are shown in Table 2-2 and those for electromechanical auxiliary storage
devices are shown in Table 2-3. Solid-state electronic and magnetic
devices are applicable to registers and high-speed control memories,
main internal memories, and on-line auxiliary storage while electro-
mechanical storage devices are applicable primarily to large capacity
on-line auxiliary storage and off-line auxiliary storage. Some off-line
auxiliary storage devices, such as magnetic tape units, are also con-
sidered input/output equipment. In fact, the distinction between off-line
auxiliary storage and input/output equipment is somewhat gray, based
largely upon whether it is used to store information generated by the
processor for its later use or whether it is used to enter data initially
into the system from the outside world or to transfer data from the
system to the outside world.

The costs of storage will vary with speed and capacity and the particular
technique employed. Typical costs anticipated by 1970 for given cate-
gories of storage, including the storage media and all mechanical and
electronic components necessary to provide an operating memory, are:

       Registers and high-speed control memory - 2 to 5¢ per bit.

       Main internal memory - 1 to 3¢ per bit.

       Solid-state random access on-line auxiliary storage - 0. 2 to
           1¢ per bit.

       Electromechanical on-line auxiliary storage - 0. 001 to 0. 01¢
           per bit.

       Photographic on-line auxiliary storage - 0. 005 to 0. 0005¢ per bit.

There is a strong likelihood that integrated circuit arrays will quickly dominate the register and high-speed control memory area. Both plated wire and etched-permalloy-toroid memories appear promising for large capacity random access "mass" memory applications.

The characteristics anticipated for solid-state storage devices in 1970 are shown in Table 2-2 and those for electromechanical auxiliary storage devices are shown in Table 2-3. Solid-state electronic and magnetic devices are applicable to registers and high-speed control memories, main internal memories, and on-line auxiliary storage while electromechanical storage devices are applicable primarily to large capacity on-line auxiliary storage and off-line auxiliary storage. Some off-line auxiliary storage devices, such as magnetic tape units, are also considered input/output equipment. In fact, the distinction between off-line auxiliary storage and input/output equipment is somewhat gray, based largely upon whether it is used to store information generated by the processor for its later use or whether it is used to enter data initially into the system from the outside world or to transfer data from the system to the outside world.

The costs of storage will vary with speed and capacity and the particular technique employed. Typical costs anticipated by 1970 for given categories of storage, including the storage media and all mechanical and electronic components necessary to provide an operating memory, are:

  Registers and high-speed control memory - 2 to 5¢ per bit.

  Main internal memory - 1 to 3¢ per bit.

  Solid-state random access on-line auxiliary storage - 0.2 to
   1¢ per bit.

  Electromechanical on-line auxiliary storage - 0.001 to 0.01¢
   per bit.

  Photographic on-line auxiliary storage - 0.005 to 0.0005¢ per bit.

Type of Storage	High-Speed Control and Scratchpad Memories		Main High-Speed Internal Memories		Solid-State On-Line Auxiliary Storage Devices		Comments
	Typical Capacity (Words)	R/W Cycle Time	Typical Capacity (Words)	R/W Cycle Time	Typical Capacity (Words)	R/W Cycle Time	
Monolithic Int. Ckt. Arrays	256	50 ns	8×10^3	0.2 us			Most promising for very high speed registers and control memories.
MOS Arrays	1,024	150 ns	16×10^3	0.6 us			Promising for low cost intermediate capacities; Volatility is disadvantage.
Planar Thin-Film	512	75 ns	64×10^3	0.2 us	2×10^6	1 us	Promising for control, main memories, perhaps on-line aux. storage.
Monolithic Ferrite	512	150 ns	64×10^3	0.5 us			Reasonable yields not proven for capacities over a few hundred words; Actively pushed by only one company.
Plated Wire	1,024	100 ns	128×10^3	0.3 us	4×10^6	1 us	Very promising in all categories.
Magnetic Core Matrix	1,024	300 ns	64×10^3	0.5 us	2×10^6	3 us	Well established and will be dominant for several years; Will be replaced eventually by batch-fab techniques.
Etched-Permalloy-Toroid			128×10^3	1.3 us	4×10^5	35 us	Promising for very low cost but reasonable yield must be proven. Actively pushed by only one company.
Continuous-Sheet Cryogenic					20×10^5	5 us	Feasibility still unproven; Not economic for capacities below appx. 10^8 bits because of refrigerant cost.
BORAM					10×10^6 (serial)		In research stage; Concept promising for low cost block-oriented aux. storage; High density feasibility not proven.

STORAGE DEVICE CHARACTERISTICS ANTICIPATED IN 1970

Table 2-2

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Type of Device	Capacity Per Unit In Char.	Average Access Time	Data Transfer Rate Ch/Sec	On-Line or Off-Line Storage	Comments
Fixed-Head Magnetic Drums	30×10^6	15 ms	700,000*	On-Line	Limited Capacity; Fast access time but high cost; Large physical volume; Proven by field use for years.
Moving-Head Magnetic Drums	300×10^6	60 ms	500,000*	On-Line	Large physical volume; Proven by field use for years.
Fixed-Head Disc Files	150×10^6	15 ms	700,000*	On-Line	Fast access time but high cost; Relatively new with limited field experience.
Moving-Head Disc Files	1500×10^6	60 ms	500,000*	On-Line	Extensive field experience; Best cost, capacity, and access time compromise.
Removable Disc Files	70×10^6	80 ms	500,000*	Either	Relatively new but widely accepted; Field experience is building up rapidly.
Magnetic Tape Loop	30×10^6	80 ms	400,000	Either	New and relatively unproven in the field; Made by only one company at present.
Magnetic Tape Reel	70×10^6	(serial)	400,000	Off-Line	Well established and proven for many years; Lowest cost per character off line; Serial access.
Magnetic Card Files	$1,500 \times 10^6$	200 ms	600,000	Either	Available several years, but not as well established as discs. Lower cost per char. for large capacity.
Optical Discs	200×10^9	Seconds	700,000*	Either	New and unproven by field use; Offered by only one company at present; Read-only; Largest capacity and low cost per character; Very slow access.

*Based on reading characters bit serial from a single track.

ELECTROMECHANICAL AUXILIARY MEMORY CHARACTERISTICS ANTICIPATED IN 1970

Table 2-3

The concept of storage hierarchies is very important in considering
the use and capabilities of storage devices. There is no one ideal
type of storage that fulfills all requirements while providing the
maximum speed and capacity for the minimum cost.

It will be necessary to use a combination of storage devices utilizing
the best characteristics of each to effect a better over-all storage
system. This is true not only within the processor itself and between
the internal and external storage but also with respect to different
levels of external storage. One important aspect in the efficient use
of hierarchial storage that should be emphasized is the need for develop-
ment of machine organization and software techniques that make the
entire internal and on-line auxiliary storage appear as a single uniform
storage to the user.

In the past few years, relatively large development efforts have been
expended on associative memories that can address stored information
on the basis of a portion of its contents rather than a unique numeric
address. Data is located by association rather than by physical location.
Basically, an associative memory involves sufficient logical capability
to permit all memory locations to be searched essentially simultaneously -
i. e. within some specified memory cycle time. The search may be made
on the basis of the entire contents of each location or upon the basis of
selected bit positions of each location. Searches may be made on the
basis of equality, greater-than-or-equal-to, between limits, less-than-
or-equal-to, and in some cases more complex criteria.

Associative memories developed to date are significantly more expensive
than random access memories having comparable capacity and cycle time.
In some types of applications the ability to address the memory by con-
tent may offer overall systems economies or speed improvements that

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justify the cost of this type of memory. However, most of these advantages can usually be obtained by using a relatively small associative memory in conjunction with a large capacity random access memory. Hence, it is not likely that a central processor will utilize a large associative memory as the main internal memory unless some unforeseen breakthrough in associative memory technology is achieved. On the other hand, small associative memories used in conjunction with large random access memories may offer advantages in tactical data systems that will justify their cost. Such uses might include track while scan, threat evaluation, and weapon assignment applications.

Read-only memories appear useful primarily for micro-program machine organizations or applications where it is necessary to emulate the instruction set of a large machine on a small machine. These techniques have been used in several recent commercial computers to provide program compatibility between different size machines in a "family" or compatibility with a competitor's system. There is no indication at this time that such requirements will exist in future naval tactical systems, but read-only memories will be available to the systems planner should he have a need for them. Possibly a more likely application may be for storing recovery programs in a multi-computer system to permit rapidly transferring into or out of a "degraded" mode of operation in the event of a malfunction in one of the computers in the system.

2.3.2 Recommendations

Magnetic core memories will continue to dominate the memory field for the next few years but batch-fabricated memory technologies, which are progressing rapidly, will ultimately replace discrete cores in most applications. The memory function is particularly adaptable to batch-fabrication techniques since it consists of large numbers of similar elements and is highly repetitive. Hence, the development of batch-

fabricated memory technologies should be emphasized wherever possible.
Batch-fabricated memories should be used in future Naval systems as rapidly
as they become technically and economically feasible since significant
advantages in cost, speed, size, and power requirements will accrue
from the use of batch-fabricated memory technologies.

Monolithic integrated circuit arrays and magnetic thin-film memories are
already being used commercially for scratchpad and high-speed control
memories. New commercial computers using thin-film and plated wire
memories for the main internal memories have been announced. Feasi-
bility models of a large capacity plated wire memory, an etched-permalloy-
toroid memory, and an interim BORAM device have been demonstrated,
and these technologies should be available for production by late 1968 for
solid-state on-line auxiliary storage. Although magnetic core memories
will remain dominant through at least 1970, some of these batch-fabricated
memory technologies should be making significant inroads into all memory
application areas by 1970.

Very large capacity on-line auxiliary storage will continue to require
electromagnetic devices such as magnetic disc files or magnetic card
memories for the forseeable future -- particularly for capacities of 10^9
bits and above. BORAM devices may ultimately cut into this application
area, but this will not occur on an economic basis until well after 1970.
However, for tactical military systems, environmental and maintainability
advantages will dictate the use of BORAM devices at the earliest possible
date -- even justifying some cost premiums. Plated wire and etched-
permalloy-toroid memories can be available for on-line auxiliary storage
for capacities of 10^8 bits prior to 1970. Firm requirements for such
solid-state mass memories and BORAM devices should be stated by the
Navy to stimulate industry in the development of these technologies and
to assure that their development is carried to the production stage.

The major contenders for different categories of future memories are:

 For discrete bit storage and registers:
  Monolithic integrated circuits*

 For high-speed control or scratchpad memories:
  Monolithic integrated circuit arrays*
  MOS arrays*
  Planar magnetic thin films
  Plated wires

 For main internal memories:
  Planar magnetic thin films*
  Plated wires*
  Magnetic cores

 For solid-state on-line auxiliary storage:
  BORAM devices*
  Plated wire*
  Etched-permalloy-toroid*
  Continuous-sheet cryogenic

 For electromechanical on-line auxiliary storage:
  Magnetic disk files*
  Magnetic card files

 For off-line auxiliary storage:
  Removable-media disk files*
  Magnetic card file cartridges
  Magnetic tape*

Those marked above with an asterisk are considered to be the most likely
candidates for future naval tactical systems, but the progress and success
of development efforts presently underway should be monitored closely
during the next two to three years to assure the selection of an individual
type of memory in each category that will best meet Naval requirements
in the 1970-1980 era. Optical storage will be another strong contender
for very large capacity on-line and off-line auxiliary storage when reversable
recording media are developed that permit alterable (read/write) storage.

Associative memories will be available in 1970 but their use should depend upon development of specific requirements in naval systems. The use of relatively small capacity associative memories in conjunction with main high-speed random access internal memories will offer some advantages, but it is doubtful that large capacity associative memories can be justified as a main internal memory in this time frame.

In summary, the following recommendations are made concerning memory technology:

1. Incorporate batch-fabricated memories in future naval systems as rapidly as they become technically and economically feasible.

2. Closely follow progress in those memory technologies recommended in the list on the preceding page to select the type memory in each category that best meets requirements for naval tactical systems in the 1970-1980 era.

3. It is not necessary for the Navy to support the development of registers, high-speed control (scratchpad) memories or main internal memories since the semiconductor and computer industries will progress rapidly in the development of new memory technologies in these categories without government support.

4. Navy or other government support is needed to assure the availability of random access mass memories (e. g. 10^8 bits) and BORAM devices for solid-state on-line auxiliary storage.

5. Navy or other government support is needed to assure the availability of improved militarized electromechanical mass memories and removable media BORAM devices for very large capacity on-line and off-line storage applications.

6. The development of optical storage techniques utilizing reversable recording media should be supported by the Navy

or other government agencies to assure the eventual availability of a higher performance replacement for large capacity electromechanical magnetic surface storage devices that would have fewer moving parts than present. devices.

7. Systems concepts utilizing small associative memories should be encouraged if they offer improvements in specific Naval requirements, but the use of large capacity associative memories as the main internal memory in this time frame is very questionable.

8. Read-only memories will be available for Naval applications, but their use should depend upon machine organization and system design requirements.

9. On-line system design concepts utilizing large capacity, solid-state, batch-fabricated memories to minimize the need for conventional electromechanical input/output equipment should be encouraged.

2.4 DISPLAYS

Batch-fabrication is a goal in searching for better display technologies, but the prospects are not as promising as in the case of logical circuits and memories. Flat panel displays are more suitable to batch-fabrication techniques; hence, flat panel displays are favored. A flat panel display is also desirable from the application standpoint for large-screen applications and to provide smaller volume console displays. Although the cathode-ray tube is expected to remain dominant at least until 1970, flat panel displays will become feasible and available for console applications in the early 1970's.

The possibility of a higher degree of compatibility with integrated circuit and other batch-fabrication technologies is an important criterion in considering technologies for future displays. This requires display

technologies that can operate with low voltage and low power. The integrated circuit techniques discussed in the component and packaging section of this report will be directly applicable to most of the electronic portions of future displays. Monolithic circuits will be used for the straight digital portions (e. g. control logic). Hybrid monolithic/thin-film circuits may be used for other portions (e. g. video amplifiers) in which linear circuits are required. Batch-fabricated memories will provide the necessary buffering and local storage capability in displays.

In the display technology portion of the 1964 ANTACCS study, primary emphasis was placed on large screen displays because of the lack of an adequate existing technology in that area and because of the acceptability of existing cathode-ray-tube console displays. Investigation of large screen display technologies was continued during the study, but an added emphasis was placed on technologies that offer a potential for reducing the size, weight, volume, and power requirements of console type displays for future tactical data systems.

Reducing the size of console displays will significantly reduce the space required on shipboard for a tactical data system. A major portion of the total space required for the present NTDS is occupied by display consoles. Flat panel displays will permit reductions in excess of 509 in the volume of NTDS type operator consoles.

During this study particular attention was given to those display technologies for 1970 era systems that appeared most promising during the 1964 ANTACCS study including:

> Photochromic displays with cathode-ray tube or laser image generation

> Thermoplastic and photoplastic light valves with cathode-ray tube or laser image generation

Crossed-grid electroluminescent displays with integrated storage

Laser inscribing systems

Cathode-ray-tube displays

Consideration was also given to other promising display technologies whose feasibility appeared questionable during 1964. This category included:

Solid-state light valves

Opto-magnetic displays

Laser/luminescent (or electroluminescent) displays

Injection electroluminescence matrix displays

Of this latter group, opto-magnetic and injection electroluminescence displays are of special interest because of their compatibility with semiconductor integrated circuits and their suitability to batch-fabrication. Feasibility models of opto-magnetic displays have been demonstrated and production units should be available within three years. Injection electroluminescence matrix displays appear very promising from a longer range standpoint.

Brighter screen cathode-ray tubes are being developed to permit use of display consoles under normal ambient light. However, the major problems and difficulties with CRT console displays have not been with the basic display technology but rather with the equipment design system operational concepts and functional design. That is. the major questions with respect to console displays are not questions of hardware technology but rather of systems design and user requirements. For example. some scan rates or frame rates have limited brightness more than the basic CRT characteristics.

Display technologies were investigated by discussions with technical experts working in these fields. by studying the applicable literature. and by evaluating information concerning the different technologies in relation

to the requirements that will be imposed by future naval tactical systems. The effect of new technologies on reliability and maintainability and their compatibility with integrated circuits and new memory technologies were given major weight in their evaluation.

2. 4. 1 Technical Summary

There has been little change in the status or expectations for most of the types of large screen display technologies investigated during the ANTACCS study in 1964. However, photochromic/CRT displays that were considered promising do not appear to have received the level of development effort that had been anticipated. This is not entirely because of technical problems, but is partially a function of the interest and goals of the companies involved. However, photochromic displays are still considered a promising technology. Photochromic glass that has been developed recently promises to overcome some of the major problems (e. g. fatigue) of the older organic photochromic materials.

In general, the conclusions and recommendations concerning large screen displays made during the ANTACCS study in 1964 remain valid. Thermoplastic and photoplastic light valves, photochromic displays, electroluminescent displays, laser inscribing systems, and opto-magnetic displays appear to be the best prospects for large screen displays by the early 1970's. Solid-state light valves, laser/luminescent displays, and injection electroluminescence matrix displays offer promise if feasibility is proven.

Unfortunately, display technology, as well as that in other input/output areas, has not kept pace with advances in digital electronics and magnetics technologies. The term "display technology" in the sense used here refers to the presentation or generation of the actual visual image (i. e. the visual transducer) rather than to the many digital logic, storage, and control circuits used in display equipment. Integrated circuits are being used now to implement these latter digital functions in newer display equipments.

Integrated circuit techniques are most effective for the implementation
of low voltage, low power, low precision components which are ideally
suited to the fabrication of bi-valued computer logic and storage elements.
These techniques are very poorly suited to the requirements of most of
the approaches to the implementation of visual transducers in use today.

Criteria for compatibility with batch-fabricated computers include low
voltage, low power, small volume, digital selection, high reliability and
long life, low cost, adaptability to batch-fabrication, and feasibility. It
is fairly obvious that the development of large-screen displays meeting
all these criteria is unlikely in the near future. However, there are
several visual transducers in research or development stages at this
time that offer promise for console displays meeting these criteria. Some
of these will later be adaptable to large-screen displays.

Most of the technologies for large-screen displays cited in Volume V of
the ANTACCS Final Report do not meet the criteria for compatibility
with integrated circuits and other batch-fabricated electronic and magnetic
components. There is no certainty at this time that any large-screen
display technologies capable of meeting these criteria will be available
by the early 1970's, but opto-magnetic displays appear promising. For
console displays there is more hope of achieving reasonable compatibility
with batch-fabricated electronic and magnetic components by replacing
the cathode-ray tube with a flat panel, low voltage, low power visual
transducer such as an opto-magnetic panel or an injection electroluminescence
matrix panel. Table 2-4 rates compatibility with batch-fabricated computers.

The cathode-ray tube represents a well established technology that
will probably be dominant for consoles into the early 1970's. The
cathode-ray tube is adequate and satisfactory from most standpoints,
but it has some disadvantages. While these are not critical, they will

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Display Technology	Relative Use As A		Compatibility With Batch-Fabricated Computers	Color Capability	Feasibility	Reliability and Life
	Large Screen	Console				
Cathode-Ray Tube	Poor	Best	Poor	Color tube can be used	Readily available	Good
Mechanical Inscribing Systems	Good	No	Poor	Filters and multiple projectors	Readily available	Poor
Film Projection Systems	Good	Possible	Poor	Filters and multiple projectors; lenticular film	Readily available	Poor
Photochromic-CRT Display	Good	Possible	Poor	Filerts or different color photochromes	In prototype stage	Good
Oil-Film Light Valves	Good	No	Poor	Filters and multiple systems	Available	Poor
Thermoplastic and Photoplastic Light Valves	Good	No	Poor	Filters and multiple systems	In prototype stage	Good

CAPABILITIES OF DISPLAY TECHNOLOGIES

Table 2-4

Display Technology	Relative Use As A		Compatibility with Batch-Fabricated Computers	Color Capability	Feasibility	Reliability and Life
	Large Screen	Console				
Solid State Light Valves	Good	No	Fair	Filters and multiple systems	Uncertain	Unknown
Electroluminescent Displays	Good	Good	Fair	Multiple-dot color using different color phosphors	By 1970	Fair
Opto-Magnetic Displays	Good	Good	Good	Color is a function of reflection angle	By 1970	Good
Laser Inscribing Systems	Good	No	Fair	Filters and multiple projectors	By 1970	Good
Laser-Luminescent Displays	Good	Possible	Fair	Unknown	Promising	Unknown
Injection Electroluminescence Matrix	Good	Good	Good	Unknown	Promising	Unknown

CAPABILITIES OF DISPLAY TECHNOLOGIES

Table 2-4

(Continued)

justify the utilization of other display technologies when these have proven feasible. The major disadvantages of cathode-ray tubes are those associated with their incompatibility with new solid-state batch-fabrication technologies. These disadvantages include physical volume, less reliability, high power requirements, and a need for high voltage circuits. In some applications involving high ambient light conditions, the brightness and contrast offered by cathode-ray tubes may also be considered limitations.

Although cathode ray tubes remain by far the dominant technology, many other approaches are being taken to implementing visual transducers. Most of the research and development work on display technology is pointed toward large-screen displays because of the inadequacy of present techniques. However, there is also interest in improved technologies for console displays that will permit a flat panel display (visual transducer) that is compatible with integrated circuits and other batch-fabrication technologies for addressing, selection, and control. The more important or more promising display technologies presently in use or in the research and development stage are compared in Table 2-4.

The difficulty of establishing quantitative measures of display system effectiveness is one of the major problems in the display field which makes comparison of widely different technologies very difficult. The columns in Table 2-4 referring to the use as large-screen or console displays is a relative one. For example, since the CRT is so satisfactory as a console display many of the other technologies are not relatively well suited to console displays; on the other hand, since none of the large-screen techniques are entirely satisfactory several of them can be considered good on a relative basis. These two columns do not refer to performance but merely to their suitability for large-screen or console images. For example, mechanical inscribing systems and film projection systems are good ways to generate large-screen images, but they are both slow and have other disadvantages compared to some of the other technologies shown.

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In considering comparisons of display technologies, it is important to remember that the selection of an appropriate display technology is not made on the basis of one or two characteristics but rather on the composite ability of the technology to best meet the needs and requirements of the specific application. A systems designer will give greater or lesser weight to individual parameters depending upon the requirements of his specific application. It is necessary to make compromises in some characteristics in order to accept a display technology that meets other essential requirements more important to the particular application.

2.4.2 Recommendations

Mechanical inscribing and film projection systems are the major large-screen display technologies available today. However, these approaches to large-screen displays suffer from problems of size, cost, reliability, maintainability, and cost of the expendable media. Hence, although these are the only practical techniques available today on a production basis, they will be replaced by newer technologies within the next few years. These promising newer technologies for mechanizing the visual transducer portion of display systems in the future include:

        Cathode-ray tubes

        Photochromic-CRT displays

        Thermoplastic, photoplastic, and solid-state light valves

        Electroluminescent displays

        Opto-magnetic displays

        Laser systems

        Injection electroluminescence matrices

Not only are CRT's the dominant technology for console displays at present, but they also play an important role as the image generator in a number of large-screen display technologies. For example, in a film-based projection system for large-screen displays the image is initially

generated on a small high precision CRT prior to its transfer to a photographic media. However, cathode-ray tubes should be replaced in naval tactical systems by flat-panel, solid-state displays as soon as some of these new technologies prove feasible for production and field operation.

Preferred display systems are those compatible with solid-state electronic component technology and those employing such components. On this basis, of the technologies presently in the research and development stage, the more promising include crossed-grid electroluminescent panels with integrated storage, matrix controlled opto-magnetic panels, and injection electroluminescence matrices. If they prove feasible, the latter two offer the greatest promise with respect to meeting the compatibility criteria set out above. Digitally deflected laser/luminescent systems may be less compatible but offer promise for large-screen displays. Electroluminescent panels and laser deflection presently require high voltages that may limit their use if other techniques more compatible with the voltage capabilities of integrated circuits prove feasible and economical.

It is, of course, very likely that presently unforeseen developments will permit additional display approaches during the 1970's, but those listed above are the most promising of the presently known technologies for providing compatibility with low-cost, high-performance, batch-fabricated computers of the early 1970's.

In summary, the following recommendations are made concerning display technology:

1. Display technologies that are amenable to batch-fabrication and that are compatible with batch-fabricated electronic and magnetic components should be emphasized.
2. Development of flat-panel visual transducers should be supported for both large-screen and console displays.

These flat-panel displays should:

    Be addressed digitally

    Provide storage inherent to the display panel

    Be compatible with batch-fabricated electronics
        and magnetics.

3. Flat-panel visual transducers and batch-fabricated electronic and magnetic components should be utilized to the greatest extent possible in console displays to achieve significant reductions in physical size of the equipment since display stations presently occupy a major portion of the floor space required on shipboard for naval tactical systems.

4. Progress in those display technologies recommended on the two preceding pages should be followed closely to select the type of visual transducers that best meet requirements for console and large-screen displays in the 1970-1980 era.

5. Navy or other government support is needed to assure the availability of large-screen displays that are suitable for dynamic real-time operation in naval tactical systems.

6. User requirements for console displays should be better defined and more efficient computer software should be developed for display functions.

2.5   INPUT/OUTPUT

Progress in input/output equipment during the next 4 to 8 years will be less than that in any of the other major areas of hardware technology covered in this study. Since present types of input/output equipment rely heavily on electromechanical techniques which are not amenable to the batch-fabrication technologies that will have major impacts on other hardware components of future systems, input/output will constitute the major hardware problem for the foreseeable future.

There are three major approaches to improving the performance of future systems with respect to input/output capability. These are:

Improvements in the performance of present types of input/output equipment.

Development of new types of input/output equipment that are not in widespread use at present.

Development of system organization concepts and techniques that minimize the need for conventional input/output equipment.

Each of these approaches will play a part in performance improvements in future systems. However, unless much greater effort is placed upon the development of non-mechanical input/output equipment, the best hope for future systems lies in developing system techniques that minimize the need for conventional types of input/output equipment. A primary example of this is the greater utilization of on-line systems in which data enters the system directly in machine language as it is generated (e. g. on-line keyboards, A-D converters, etc.) and data is supplied directly to its final destination (e. g. on-line CRT displays, D-A converters, etc.), thus eliminating electromechanical intermediate devices such as punched tape, punched cards, or magnetic tape handlers.

During this study, emphasis was placed on the investigation of new i. ut/output techniques that offer promise for performance improvements in future systems - particularly ones which were not covered in detail in the 1964 ANTACCS study. These investigations have included:

Character recognition and print readers

Voice recognition and voice output

Non-impact printers

Non-mechanical keyboards

Incremental magnetic tape

Solid state replacements for magnetic tape equipment

New devices and techniques, both in the research stage and currently under development, to allow direct entry of data were investigated and evaluated. The investigation and follow-up of particularly interesting new techniques and approaches that were examined during the initial ANTACCS study and improvements in conventional types of input/output equipment were continued. New forms of graphic input equipment, new types of graphic output equipment, digital-to-analog and analog-to-digital conversion equipment, and trends toward the replacement of analog data generating equipment with digital data generating equipment were also examined.

2.5.1 Technical Summary

Almost all present types of input/output equipment are electromechanical. This imposes limitations on the improvements that can be achieved and on the ability to utilize the benefits of batch-fabrication techniques in electronics and magnetics. Although these electromechanical input/ output equipments will limit systems performance, the effect on systems costs and reliability is even more serious. The performance limitations could be overcome to some extent by using a larger number of input/output units, but this further accentuates the cost and reliability imbalance with respect to the central processor and memory.

Performance characteristics anticipated by 1970 for some of the major types of conventional input/output equipment are shown in Table 2-5. Examination of these characteristics indicate performance improvements of less than one order of magnitude and in most cases of less than two-to-one over equipment commercially available today. Punched paper tape is not included in Table 2-5 because it is believed that incremental magnetic tape readers and recorders will replace punched paper tape equipment for most high performance applications.

Magnetic tape units	300,000-400,000 char/sec read write rate	2000-3000 char/inch density
Incremental magnetic tape		
Recorders	800-1000 char/sec record rate	800 char/inch density NRZI
Readers	500-600 char/sec read rate	800 char/inch density NRZI
Punched cards		
Punches	500-700 cards/min punch rate	
Readers	2000-3000 cards/min read rate	
Line printers		
Impact type (multiple copy)	2000-2500 lines/min	*64 character type font
Non-impact type (single copy)	5000-7000 lines/min	*64 character type font

* Larger type fonts will be available at slower rates.

INPUT/OUTPUT EQUIPMENT CHARACTERISTICS
ANTICIPATED BY 1970

Table 2-5

Incremental magnetic tape equipment will be cheaper for high performance, will be more reliable, and will utilize tape records and formats that are completely compatible with high-speed conventional magnetic tape units. Although block oriented magnetic tape units have been in use since the early days of the computer industry, the ability to economically read and record incrementally opens new applications for magnetic tape input/output.

Incremental magnetic tape recorders and readers offer definite advantages as replacements for punched paper tape equipment, but they also have some unique applications made possible by the combination of asynchronous read and write rates and compatibility of tape formats, speeds, and densities with conventional computer magnetic tape equipment. Thus, a tape recorded asynchonously on an incremental recorder can be read as computer input on a conventional tape transport and an output tape prepared by a computer can be read asynchronously on an incremental reader. The use of higher density and reusable magnetic tape will eliminate the logistics problem of keeping military punched tape equipment supplied with expendable paper tape and will minimize operator time required to change reels.

Rapid progress is being made in the development of non-impact printers in which moving parts are reduced to a minimum. The inability of non-impact printers to satisfactorily produce multiple copies has been a major disadvantage, but their advantages over conventional electro-mechanical printers in minimizing maintenance, power, space, weight, and noise are significant for military applications. The problem of obtaining multiple copies can be overcome to a large extent by the use of improved copying machines producing inexpensive dry copies which are in widespread use in the commercial field. Non-impact printing techniques using electro-optical, electro-graphic, magnetic, electro-chemical, photo-chemical, and ink spray techniques have been under development.

Several development efforts are underway directed toward replacing the conventional punched card as a unit record with either a printed card or a magnetic card. The goals of these developments are to provide a discrete unit record media that does not cause the problems inherent in mechanically punching holes in a card. There is some question about the real need for a unit record device of this type in military applications, but the Army Engineering Laboratory at Ft. Monmouth is quite interested in improved unit record devices - particularly for logistics type applications. The advantages of unit record devices for NTDS type systems are less clear. These types of devices probably will not play an important role in future naval tactical systems.

Improved graphic input devices to provide inputs that are readily compatible with displays are of extreme importance to future naval tactical systems. The ball cursor used in the present NTDS console may eventually be replaced by newer devices such as an improved light pen, or a RAND Tablet. Conventional light pens and newer devices of a similar nature, such as the beam pen, are not as attractive for future naval applications as the RAND Tablet, which enters positional data directly in digital coordinates. The RAND Tablet is not necessarily (but may be) directly associated with the face of a cathode-ray tube as light pens must be. For example, the surface of the RAND Tablet can be on the horizontal face of a table facilitating drawing on the surface, while the cathode-ray tube is in a semi-vertical position. This also avoids the problem of interposing the viewer's hand, which would be necessary to hold a light pen, between the viewer and the display. The output of the Tablet can easily be used to generate a spot on the face of the cathode-ray tube to indicate the equivalent position of the pointer on the Tablet, thus permitting easy correlation between the display and the graphic input surface. The Tablet permits a higher resolution than is available with either the light pen or the

beam pen. · The ability of the RAND Tablet to operate while disassociated from a cathode-ray tube screen, makes it attractive as a graphic input device for use with large-screen displays. A transparent Tablet can easily be superimposed over the face of the cathode-ray tube if this is desirable. The ability to position the RAND Tablet in a convenient location and attitude independently of the display screen, can be important in some military applications where the display itself may be viewable to the user but inaccessible to his hands.

The batch-fabrication techniques that are expected to significantly improve digital electronics are also applicable to analog-to-digital and digital-to-analog converters. Hence, these devices will be available at lower costs, higher reliabilities, and smaller sizes in the future. Increased use of analog-to-digital and digital-to-analog converters operating directly on-line with the computer will aid in achieving the minimization of conventional electromechanical input/output equipment (e. g. punched cards, punched tape, magnetic tape, etc.) discussed previously. The availability of high reliability, low-cost devices of this type will be another step toward the goal of capturing the maximum amount of data at its source and delivering it to its destination without intermediate operations.

From a somewhat longer range standpoint, character recognition, non-mechanical keyboards, solid-state replacements for magnetic tape equipment, and voice output will provide non-mechanical replacements for conventional input/output equipment. Eventually, voice input will do the same, but from a much longer range standpoint.

Low cost batch-fabricated logic and storage components will make possible significant reductions in cost and improvements in reliability of character recognition equipment. This equipment can, in turn,

eliminate the need for manual keyboard transcriptions from printed information to machine language using intermediate devices such as tapes or cards. Character recognition equipment can be useful in a military system by permitting data prepared on simple printers (e. g. a typewriter) at remote locations to later be used directly as computer input. This eliminates the necessity of either placing relatively expensive and bulky equipment at the remote location for producing machine language data or of transcribing the printed information by manual key-punch operations at the computer location. It also minimizes the training and skill required by the individual generating the data at the remote location permitting this to be done by anyone using a "hunt and peck" system on the typewriter. The development of character recognition equipment to the point that it becomes feasible to read constrained hand printed characters will further facilitate the ability to generate computer input data at remote locations without special equipment and with minimum training. This should be very advantageous for naval tactical systems - particularly Marine Corps systems in which data may originate from isolated groups.

From a much longer range viewpoint, batch-fabrication will also make feasible voice input which will require large amounts of batch-fabricated logic and which will eventually provide a direct input means from the human to the computer. Limited voice output equipment is already available and in use. More sophisticated voice output equipment is anticipated. Voice input and voice output is of particular importance in military applications because of the ability to input and output data from and to remote sources using conventional voice communication equipment that is already widely available in military operations. Input data could be received or output data sent to remotely located users on shipboard using the conventional telephone system. This may be even more important in Marine Corps operations where

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conventional radio communications equipment could be used for providing communications between the computer and remote observation posts or small isolated units. Voice output equipment capable of providing output information, such as warnings of fire patterns or enemy action, to remote isolated units can easily be provided with state-of-the-art technology available today.

Non-magnetic keyboards will further minimize the number of mechanically moving parts in the system and can facilitate the manual input/output operation by permitting more design freedom in the keyboard from a human factors standpoint. Eliminating the need for mechanical linkages will permit locating the keys in a configuration that is more adaptable to the convenience of the human hand than the rectangular keyboard used at present. Pneumatic, optic, and piezo-electric techniques are under development for non-mechanical keyboards. Such devices have been demonstrated and are feasible now. They can be available any time the Navy is willing to re-train keyboard operators and convert to a new device that will appear ratically different to the operator. The "feel" of a conventional typewriter or teletype on which most present operators have been trained will have to be sacrificed to achieve the advantages of reliability, maintainability, and improved human factors design offered by non-mechanical keyboards.

Solid-state replacements for magnetic tape equipment have been discussed in greater detail in the memory technology portions of this report (See Section 2.3 and Appendix B). Basically the efforts to replace magnetic tape require the development of solid-state storage devices in which the storage media is very economical and can be physically removed from the read/write mechanism. The Army Engineering Laboratory at Ft. Monmouth is the major organization pushing the development of these devices, which they refer to as block-oriented-

random-access-memory (BORAM). Their goals call for 4,000,000 character removable storage modules with costs of approximately 0.015¢ per character for off-line storage. Random access to the beginning of any block in 1 microsecond, read/write rates in the order of 2 to 3 million characters per second, and power and weight requirements approximately one tenth those of conventional magnetic tape units are further goals of the program. The development of such BORAM devices at reasonable costs would have a significant impact on future naval tactical systems as a result of the improvements in reliability, maintainability, susceptibility to environmental conditions, size, and weight afforded by the use of solid-state electronic rather than electro-mechanical techniques. Performance improvements would also result from the fast random access to the beginning of a block and the high data rate. Although an interim BORAM device will be available sooner, devices possessing all of the desirable characteristics discussed above will not be available for field use until approximately 1972 to 1974.

The greatest improvement in the input/output aspects of large systems can be achieved by minimizing input/output operations wherever possible. By keeping the data within the system when it will be required for reuse and by capturing data at the source, the need for conventional input/output equipment can be reduced. For example, the need for large printed reports can be minimized or eliminated when the user is operating on-line with the processor through a display console. When the entire data base within the system is available to the user upon request, he will have little need for reports and other off-line references which may be out of date by the time they are used. The display consoles in present NTDS systems provide a good example of this approach with input and output being handled directly on-line through the user consoles. The major use of conventional types of input/output equipment in NTDS has been reduced to that of loading and changing of programs. To

achieve the improvements possible in this area in larger systems
requires a combined effort of users, programmers, hardware engineers,
and systems planners and designers.

2.5.2   Recommendations

The present types of electromechanical input/output equipment will con-
stitute the major hardware problem in future systems.   The best
approach to improving input/output aspects of future systems lies in
the development of system organization concepts and techniques that
minimize the need for conventional input/output equipment.   From the
short-range standpoint, the development of improved input/output equip-
ment of types presently available, should be continued wherever worth-
while improvements can be achieved, but there is a limit to the
improvements that can be anticipated in electromechanical equipment
of this type.   From a longer-range standpoint, it is necessary to
develop new types of input/output equipment that either eliminate or
minimize mechanically moving parts.   Input/output devices that offer
promise for minimizing mechanical motion include:

> Character recognition and print readers
>
> Voice recognition and voice output
>
> Non-impact printers
>
> Non-mechanical keyboards
>
> Incremental magnetic tape as a replacement for punched
> tape or cards
>
> Solid-state replacements for magnetic tape equipment

The present NTDS system is one of the best existing examples of
systems design in which the need for conventional electromechanical
input/output equipment has been minimized by on-line systems
operation.   This approach should be extended further by using large
capacity on-line auxiliary storage to store alternate programs to

further reduce the magnetic tape and punched paper tape usage. Solid-state auxiliary storage devices should be utilized as soon as economically feasible. When low cost solid-state on-line auxiliary storage is available, it should be utilized also in conjunction with operator display consoles to minimize printing requirements. Serious consideration should be given to the use of available voice output techniques in the near future to permit the use of conventional voice communication facilities for making computer outputs available to remote parts of a ship or to remote or isolated Marine Corps units.

In summary, the following recommendations are made concerning input/output technology:

1. Emphasis should be placed on system design concepts that minimize the need for conventional electromechanical input/output equipment.

2. Improvement of present types of input/output equipment should be encouraged, but such efforts should be funded by the Government only where significant improvements can be achieved or where there is a pressing need for a particular type of equipment on a time scale that cannot be met by any of the other approaches recommended here.

3. Development of new types of input/output devices that minimize mechanically moving parts, particularly those recommended on the preceding page, should be supported by the Navy for use in systems to become operational in the 1970 to 1980 era.

4. Presently available voice output techniques should be utilized by the Navy and Marine Corps for supplying computer output over existing communication links directly to remote or isolated locations.

5. Non-impact printers, non-mechanical keyboards, and incremental magnetic tape which are feasible, and in some cases available, today should be utilized by the Navy at the earliest possible time.

6. Systems designed to become operational in the 1970 to 1980 era should utilize large capacity solid-state on-line auxiliary storage to minimize requirements for electro-mechanical on-line and off-line storage devices.
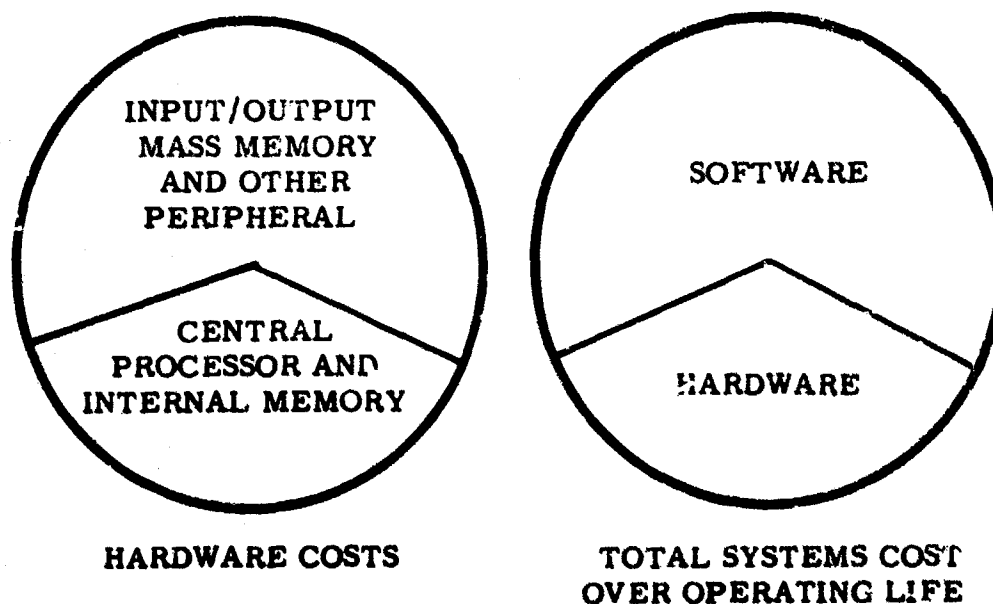
3. SYSTEMS IMPLICATIONS OF NEW HARDWARE TECHNOLOGIES

The feasibility and relative merit of advanced hardware technologies have been discussed from the hardware standpoint in Section 2 and in the Appendices. Many of them will have significant impact on the capabilities, design, and utilization of future systems. To achieve true potential offered by some of these new technologies, they must not be used as direct replacements for existing hardware in present machine organizations or system configurations. Some of these advanced technologies are so different from, or offer so much greater capability than, existing technologies that they require new concepts of machine organization, systems design, and naval utilization of computer and data processing systems. One example of this is the impact of batch-fabrication technologies on maintainability, which is discussed in greater detail in Section 4. Other systems' implications of advanced hardware technologies, the need for significant conceptual changes in future systems, and some of the problems created will be discussed in this Section.

Present computer organization and the design of computer centered systems have been heavily influenced by the high cost of electronic and magnetic hardware for mechanizing logical functions and storage in the central processor. These costs have been dropping steadily in terms of the cost per component, but increases in the complexity and capacity of central processors have tended to keep pace with decreases in hardware costs. As a result, reductions in hardware costs to date have been reflected primarily in increased performance and capability rather than reduced cost. However, developments presently underway in batch-fabricated technologies will provide such significantly lower hardware costs in the central processor that it will not be possible to maintain a system balance from the standpoint of cost and reliability. If properly

used, large-scale integrated-circuit arrays in particular will provide
digital logic and control functions at such sharply reduced costs and
increased reliability that the central processor will tend to become an
almost negligible part of the system from the standpoint of both cost and
reliability.   The dominant factors in systems cost will be software and
electromechanical mass storage and input/output devices.

In a typical large computer or data processing system at present, the
central processor and internal memory, which are most amenable to
the advantages of batch-fabrication, represent approximately 25% to 35%
of the total hardware cost in the data system.   Over a total operating
life of 8 to 10 years, the software represents 60% to 80% of the total
systems cost and the hardware only 20% to 40% of the total systems cost.
This is illustrated in the two charts below:

INPUT/OUTPUT
MASS MEMORY
AND OTHER
PERIPHERAL

CENTRAL
PROCESSOR AND
INTERNAL MEMORY

SOFTWARE

HARDWARE

HARDWARE COSTS

TOTAL SYSTEMS COST
OVER OPERATING LIFE

As a result, in reducing the cost of the central processor and internal
memory, batch-fabrication technologies will affect equipment
representing only 25% to 35% of the hardware cost, while the total hard-
ware cost represents only 20% to 40% of the systems cost.   Hence, the

central processor and internal memory represent only 5% to 15% of the total systems cost. The low level digital logic and storage portions of peripheral equipments may represent another 5% of total systems cost. Therefore, only 10% to 20% of present computer and data processing systems from the cost standpoint will be affected by batch-fabrication technologies that can be foreseen at this time.

In view of these considerations, large integrated circuit arrays and other batch-fabrication technologies will reduce the total cost of future systems by less than 20% unless research and development efforts in input/output, mass strrage, and software are greatly accelerated and breakthroughs are achieved in these areas that are presently unforeseen. To achieve the real cost potential of batch-fabrication technologies, designers of future systems will have to utilize them not only in cutting the cost of the central processor and internal memory, but also in reducing costs in other parts of the system. Hence, the three major problems facing designers of future naval tactical data systems will be:

1. The necessity of developing machine organization techniques that will permit the efficient utilization of large integrated circuit arrays and other batch-fabrication technologies to achieve their true potential in terms of cost, reliability, and maintainability.

2. An urgent need to minimize the number of electromechanical input/output and mass storage devices required in a system in order to reduce systems cost and increase systems reliability and an accompanying need for developing new and improved types of such peripheral equipments.

3. An equally urgent need for minimizing the cost of providing software, including both operating systems and user programs, even if this requires significant increases in the logical and storage hardware in the central processor.

3.1 MACHINE ORGANIZATION AND SYSTEM DESIGN CONCEPTS

In order to facilitate the use of large arrays and to minimize the inter-connections between batch-fabricated units, extensive research and development in new machine organization and system design techniques is needed. Logical design and machine organization approaches must be developed that will permit a machine to be organized along much more highly functional lines than at present so that a computer can be assembled from a limited number of relatively large functional blocks.

In considering the advantages of large integrated circuit arrays and other batch-fabrication technologies, it seems apparent that the larger the array that can be effectively utilized the better the economics and reliability up to the limit that can be achieved technically in terms of the number of components per chip.[1] The use of very large arrays will reduce the initial fabrication costs and improve reliability and maintainability, but it will also present a serious problem. As the module becomes larger it becomes increasingly difficult to use it for more than one function within a single computer. Each packaged unit tends to become unique with only a single one of each type used in a given computer. Dr. R. N. Noyce called attention to this last year and indicated the anticipated progress in array size when he stated:

> "However, from a point on the complexity scale now where 50 components is the cheapest level for an integrated circuit, I expect to move to 1000 by 1970 ... At the same time there will be new problems where it takes only 10 chips to make a computer and almost every circuit made will be different."[2]

[1] Sack, E. A., Lyman, R. C. and Change, G. Y., "Evolution of the Concept of a Computer on a Slide," Proceedings of the IEEE, Vol. 52, No. 12, December 1964, pp. 1713-1720.

[2] Noyce, R. N., San Diego Council of WEMA.

This decreased "commonality" increases fabrication costs because of the low production volume of each type of module. It also increases the cost of the spares inventory, but the cost of spares usage will decrease as a result of significantly higher reliability. In fact, the low rate of usage of spares coupled with the difficulty of repairing large arrays should lead to adoption of a "throw-away" maintenance concept where major portions of the computer are replaced but not repaired in event of failure (See Section 4). This will have significant effects on maintenance procedures and costs - particularly in tactical military systems.

The lack of flexibility in large integrated circuit arrays, which tends to make each array within a system unique, and the possible need for eliminating bad or substandard circuits from the array to achieve a reasonable yield are two of the major problems in utilizing large arrays in computers. At least three different approaches to fabricating large interconnected arrays to overcome these obstacles to their utilization are under consideration (See Section 2.2.1). These are "cellular logic"[3], "discretionary wiring" or computer control of inter-connection masks[4], and fixed mask patterns that depend upon high yields of large arrays.

In the future the last two techniques will both be used. Programmed control of the interconnection pattern will likely be used for small production volumes and unique or infrequently used functional modules. However, there is strong evidence that the semiconductor industry will produce large arrays with yields sufficiently high to permit the use of standardized interconnection patterns for functional modules

[3] Minnick, R. C., "Application of Cellular Logic to the Design of Monolithic Digital Systems," Microelectronics and Large Systems (Spartan Books, Inc., Washington, D.C., 1965), pp. 225-247.

[4] Kilby, J. S., "Device Fabrication," Proceedings of the 1966 International Solid-State Circuits Conference, p. 30.

that are used in large quantities.

As semiconductor and batch-fabrication technologies advance, the major physical limitation on the size of the functional unit will be the number of external leads that can be provided on a package. Although packages with larger numbers of leads (in the order of 100) are being developed, additional research in machine organization is needed to develop functional organizational concepts that will maximize the interconnections within a replaceable package and minimize the interconnections between packages. The way in which the computer is divided into functional modules can greatly increase or decrease the number of connections needed between such modules. [5] These functional blocks should be self contained to the greatest possible extent with a minimum number of signals passed from one functional block to another.

Such functional organizations can be achieved at the expense of quite inefficient logical design within each block since the number of logical elements within each functional block will be relatively unimportant. The number of interconnections between functional blocks will be of major importance. It will be necessary to use different criteria for design efficiency in batch-fabricated systems. In the past, minimizing the number of logical elements has been a major goal of most logical design efforts. In future systems, logical elements should be used inefficiently in order to minimize the number of interconnections between functional modules. For example, frequently in present

[5] Rice, R., "Systematic Procedures for Digital System Realization from Logic Design to Production," Proceedings of the IEEE, Vol. 52, No. 12, December 1964, pp. 1691-1702.

computers a given gate or flip-flop supplies inputs to a number of
logical elements in different parts of the machine; but in future
systems the logical gate or flip-flop may be duplicated many times in
different parts of the system to minimize the signals transferred from
one module to another. Emphasis must be placed on reducing the
number of packages and the number of interconnections between
packages - even at the expense of increasing the logical complexity
of each package significantly. The criteria for machine organization
and system design should be adaptability to batch-fabrication tech-
nologies rather than logical efficiency or minimization of logical
components.

If the machine is organized along highly functional lines as discussed
previously in order to use very large arrays, there will be a strong
tendency for each functional block to be unique in a single computer.
Hence, in order to achieve the cost and maintenance advantages
offered by the use of large batch-fabricated arrays, it will be necessary
to develop machine organization and system design techniques
that permit repetitive use of packages containing very large arrays of
circuits. One approach is to change the internal organization and
logical design of the large computer so that large functional arrays can
be used repetitively even if this means that each array is relatively
inefficient in terms of the utilization of circuits within the array.[6]

Another approach is to use very small standard modular computers
designed to be used either individually or in multi-computer systems.
In this case, the uniqueness of large functional arrays within a given

[6]Rice, R., "Integrateds - The Predictable Effects on Engineering,"
Proceedings of the National Symposium on the Impact of Batch
Fabrication on Future Computers, pp. 237-253.

computer is accepted. Such a small standard modular computer can be fabricated with a very limited number of circuit arrays each of which is used only once within that computer. For example, the complete program control unit and all of its internal interconnections may be fabricated in a single package, the complete arithmetic unit in a second package, the complete input/output control and buffering section in a third package, and storage modules in additional packages containing 2000 words each. Economics in fabrication and spares inventory would be achieved as a result of the volume usage of each type of module made possible by the use of a large number of these standardized computers rather than by the use of a large number of identical packages within a single computer. When additional computing speed and capability is required the standardized computer would be used in a multi-computer configuration.

Multi-computer systems have been under active investigation for a number of years and several successful systems have been designed on this basis. The Navy Tactical Data System, which provides for up to four computers working together on a common problem with direct data interchange, is a primary example of this type system. However, multi-computer systems to date have been limited to a relatively small number of large computers in each system. To aid in the problem of utilization of large quantities of identical batch-fabricated arrays, it will be necessary to think in terms of multi-computer systems utilizing a large number of very small standardized modular computers. This not only raises machine design problems but also severe programming problems requiring software research and development to permit the effective utilization of large numbers of small standard modular computers in a multi-computer system without prohibitive overhead costs for executive control routines.

A third approach is to develop parallel processing systems conceptually similar to those that have been discussed extensively in the literature such as the Solomon or Holland machines. [7, 8]   In this approach, large arrays are used effectively by organizing the machine on the basis of a relatively large number of identical processing modules. In these highly modular computers a given module that performs some specific function may be relatively slow but it is repeated many times in the system to provide a high over-all systems speed.

3. 2   SYSTEM IMBALANCE AND THE NEED FOR IMPROVED
         INPUT/OUTPUT AND MASS STORAGE

The most difficult problems in future systems will be encountered in the input/output and mass storage areas since most equipments of these types at present rely heavily on electromechanical techniques. As a result they are not readily amenable to the batch-fabrication techniques that will bring such significant improvements in other parts of the system. There are three major approaches to improving the performance of future systems with respect to input/output equipment. These are:

> Improvements in the performance of present types of
> input/output equipment .
>
> Development of new types of input/output equipment
> that are not in widespread use at present
>
> System organization approaches that minimize the need
> for conventional input/output equipment

Each of these approaches will play a part in performance improvements in future systems. However, unless much greater effort is

[7]Holland, J. H. , "Iterative Circuit Computers: Characterization and
   Resume of Advantages and Disadvantages, " Microelectronics and
   Large Systems (Spartan Books, Inc. , Washington, D. C. , 1965), pp. 171-178.

[8]Crane, G. A. , "Economics of the DDLM, A Batch-Fabricatable
   Parallel Processor," Proceedings of the National Symposium on
   the Impact of Batch Fabrication on Future Computers, pp. 144-149.

placed upon the development of non-mechanical input/output equipment, the best hope for future systems probably lies in developing system techniques that minimize the need for input/output equipment.

Almost all present types of input/output equipment involve electro-mechanical techniques and components to a large extent. Many also involve high voltage or high powered electronics which are not amenable to batch-fabrication technologies. This imposes limitations on the improvements that can be achieved and on the ability to utilize the benefits of batch-fabrication of electronic and magnetic components. Performance improvements of less than one order of magnitude, and in most cases of less than two-to-one, over equipment commercially available today are anticipated (See Section 2.5).

Several new types of input/output equipment are under development that offer promise for performance improvements in future systems, including character recognition, voice recognition, voice output, and graphic input and output (See Section 2.5). Some of these, such as optical character readers, are in limited use at present while others, such as voice recognition equipment, are probably ten years away. Advances in integrated circuit logic components and batch-fabricated memories will aid in making some of these economically feasible.

Solid-state replacements for magnetic tape units may improve the speed and reliability available for this type of input/output function. Cost competition with magnetic tapes is questionable, but solid-state reliability and reduced size and weight would be major advantages in tactical military systems. If solid-state storage modules that can be plugged into read-write electronics in a manner somewhat equivalent

to placing a reel of tape on a tape unit prove feasible and economical, the input/output and off-line storage functions presently provided by magnetic tape could be provided by high-speed high-reliability devices and media with no moving parts. A BORAM device of this type providing random access to a block of data in the storage module, could also be used as a replacement for electromechanical on-line mass memories.

However, the greatest improvement in the performance of the input/output aspects of the system can be achieved by avoiding input/output operations wherever possible. By keeping the data within the system, by capturing data at the source, and by delivering data directly to its destination, much of the need for conventional types of input/output equipment can be eliminated. For example, the need for voluminous printed reports can be reduced sharply if the user is operating on line with the processor through an efficient console. When any part of the data base within the system is rapidly available to the user upon request, he will have little need for large reports that are used for occasionally looking up printed results - particularly since these may be out of date by the time they are used. New graphic input devices, such as the RAND Tablet, coupled with improved low cost display panels, will further facilitate on-line man-machine communication and interaction. In general, any effort to increase the extent to which systems are "on-line" will tend to reduce the amount of conventional input/output equipment in the system. Again, the present NTDS system is a leading example of the trend toward greater on-line operation. Integration of all computing and data processing functions on shipboard into a network with automatic on-line data communication between computers in sensors, weapons systems, intelligence

systems, logistics systems, and command and control systems will not only provide better and more timely responses, but will also greatly reduce the need for conventional input/output equipment. Achieving the improvements possible in this area will require a combined effort of users, programmers, hardware engineers, and systems planners and designers.

Very large capacity mass memories represent another major problem area for future systems which is closely related to the input/output problem discussed above since similar techniques and mechanisms are used at present. Batch-fabricated electronic and magnetic technologies will provide solid-state on-line auxiliary storage with reasonably large capacities in the order of 10^8 bits. Cryogenic techniques may push this up to 10^9 to 10^{10} bits. However, for very large auxiliary storage requirements in excess of 10^9 or 10^{10} bits, electromechanical devices will be required for the foreseeable future to keep the costs within reason. Further research and development in block-oriented random-access memories (BORAM) may eventually provide a solution to this problem that will eliminate the necessity for electromechanical mechanisms with consequent improvements in cost, size, and reliability.

3.3   COST IMBALANCE AND THE NEED FOR MINIMIZING SOFTWARE COSTS

The memory capacity of early computers was so limited that programming costs were not a significant part of the total cost-of-ownership of a computer system. However, reductions in hardware costs have been accompanied by greatly increased memory capacities which have permitted the storage and operation of larger and more complex programs. The cost of hardware and the cost of engineering

design required to efficiently use expensive logical components have exerted a strong pressure in the direction of very general purpose computers which can be adapted to a large number of different operations so that design and production costs can be amortized over a relatively larger number of units. It has been recognized that a special purpose computer can perform a particular task more efficiently than a general purpose computer in terms of the amount of hardware required, but the cost of small volume production and specialized design have favored general purpose computers.

Under these circumstances, the tasks of specializing the capabilities of a general purpose computer to a specific job and adapting it to the control of a large number of different types of input/output and peripheral devices have been left to the programmer. However, the increased performance and capability of computers that have accompanied the reductions in basic hardware costs in recent years have placed greater and greater requirements on the programming necessary to adapt more sophisticated general purpose machines to more complex operations in specific kinds of problems.

While hardware costs have been decreasing, programming costs have been increasing significantly to the point that they now represent at least 50% of the initial cost of a new computer system and perhaps as much as 80% of the total systems operational cost over a 10 year period. This problem is now magnified by new batch-fabrication technologies, such as large-scale integrated circuits and plated-wire or thin-film memories, which are expected to reduce the cost of logic circuits and storage elements by 1 to 2 orders of magnitude. However, the effect of these hardware cost reductions on the cost-of-ownership (initial procurement cost and systems operational cost over the lifetime of the

system) is limited by the overwhelming software costs which will not be affected by these advances in hardware technology unless machine organization and system design concepts are changed.

Fortunately, the significant reductions that are being achieved in the cost of logic and storage offer an opportunity to also reduce the mounting cost of software by trading low-cost hardware for expensive software. Many of the functions relegated to programming in the past because of high hardware costs can be performed in the future by low-cost batch-fabricated hardware with a consequent reduction in pro-gramming complexity and costs. The designers of future naval tactical systems must take advantage of low-cost logic and storage hardware to minimize software costs. Technological changes now make it necessary to reverse the past practice of using additional software to minimize hardware requirements. In the future, additional hardware will be used to reduce programming requirements. This can only be achieved by re-evaluating the criteria used for making hardware/software trade-offs in the past.

At least three different approaches to altering previously accepted hardware/software trade-offs can be considered:

1. Special purpose computers and processors
2. Different types of machine language and machine organization
3. Additional hardware functions in machines with conventional languages and organizations

Special Purpose Computers and Processors

The major arguments against special purpose computers have been design costs and lack of flexibility. Special purpose computers have been frequently favored for applications where a relatively large number of machines have been required to do a certain set of fixed

tasks, but in most such cases some limited form of program control (e. g. paper tape, plug board, etc.) has been added to provide some flexibility. With the advent of computer aided design and computer controlled preparation of masks for large-scale integrated circuits much of the design cost obstacle is removed. In essence, the question then becomes one of trading logical design in a special purpose machine for programming in a general purpose machine. In this case, the logical design will probably win out in terms of the number of man hours required since the logical designer can address himself to the task at hand with few predesign boundary conditions while the programmer does not have a completely free hand because of the characteristics of the general purpose machine he is adapting to a specific problem.

The problem of flexibility remains, but this may be partially overcome by a compromise in a multi-computer or multi-processor system. In many cases it is not necessary that all of the processors or computers in such a system be identical nor that they all be general purpose. A multi-computer or multi-processor system is feasible in which some of the computers or processors are general purpose while others are special purpose, designed to perform specific tasks that are relatively common. For example, in a multi-computer scientific computation system one or more of the computers could be DDA's. As another example, in a multi-processor system one of the processors could be a logical processor, another an arithmetic processor, etc. It seems fairly obvious that such use of special purpose computers or processors will reduce the programming requirements (as well as probably increasing processing speeds) and will be economically feasible when the low-cost potentials of large-scale integration are realized. However, logistics and maintenance considerations may argue against this approach

for tactical military systems. The price of additional programming costs and complexity may be justified to achieve a higher degree of standardization between computers on a ship to reduce spare parts, training, and maintenance requirements.

Different Types of Machine Language and Machine Organization

Present machine languages and machine organization concepts have been heavily influenced by the cost and capabilities of specific types of hardware in the past. The storage hierarchy is one example of this. The sequential one-address machine language is another. If word size were not limited by the cost of larger registers and storage, three-address machines would undoubtedly be more prevalent, particularly in data processing type applications.

Machine languages have been designed to permit efficient implementation of the processor itself rather than to facilitate programming. Users on the other hand have developed pseudo-languages that facilitate programming from a human standpoint but that require compiling operations that do not always utilize the true capabilities of the computer. On the surface there seems to be an advantage in using some higher order language (e. g. FORTRAN, ALGOL, CS-1 , etc.) as machine languages, if hardware costs are sufficiently low. It will probably not be feasible to go this far, nor is it necessarily desirable. However, it is feasible and desirable to design machine languages that will facilitate compiling operations and to implement certain parts of problem-oriented languages in hardware. The need for better problem-oriented languages has been cited frequently.[9] This is particularly true for tactical command and control applications. Hence, a joint effort by programmers and engineers to first design better problem-oriented languages for naval tactical systems and then to implement

[9]Steel, T. B. , Jr., "Promising Avenues of Research and Development - Programming Research," Portion of panel discussion at 1965 FJCC.

portions of them (e. g. mathematical operations) with hardware where-ever possible should pay handsome dividends. With very low-cost large-scale integrated-circuit arrays just over the horizon, it should be economically feasible to implement machine languages that will eliminate many of the steps in present compiling operations. This use of low-cost batch-fabricated hardware plus improved problem-oriented languages offers the greatest promise for reducing software costs in future naval tactical systems from a long-range standpoint.

Additional Hardware Functions in Conventional Machines

It is not necessary to go as far as special purpose computers or new machine languages and organizations to achieve some significant economies in software in a shorter time span by greater, and perhaps "inefficient", use of low-cost hardware. Significant economies can be achieved within the framework of conventional machine languages and organizations by:

   Hardware implementation of special purpose functions and logical and mathematical operations.

   Implementation of hardware features that minimize "red tape" and "housekeeping" programming requirements.

   Hardware implementation of some of the machine functions presently handled by operating systems software.

Many functions presently handled by programmed subroutines can be implemented easily by special purpose logic in a straight-forward manner. Such functions include:

   Binary-to-decimal and decimal-to-binary conversions

   Code conversions

   Coordinate conversions

   Format control

   Table look-up operations

Scaling

Mathematical operations (e. g. square root, trigonometric functions, matrix operations, etc.)

In the past such functions have been handled by programmed subroutines using the machine's basic operations (e. g. add, multiply, shift, etc.) because of the cost of the hardware required to mechanize the functions in relation to the frequency of their use and because of the flexibility offered by the ability to modify the routine either as it is stored or by index registers at the time of execution. From the cost standpoint, batch-fabricated hardware, such as large-scale integrated circuit arrays, will make it feasible to mechanize such functions even when they are used relatively infrequently. The necessary flexibility can be retained by hardware mechanizations that permit program control of variable operations in such functions while still significantly reducing the software required. Hardware mechanization of functions of this type will not only reduce the programming effort and the storage space required for the program, but will also offer speed improvements since logical implementation of such functions is invariably faster than the execution of the equivalent sequence of program steps.

A large portion of most programs consist of "red tape" or "housekeeping" instructions that either are not conceptually necessary to the solution of the problem or that can be implicit to the operation performed rather than stated explicitly. These include operations such as:

Register-to-memory or memory-to-register transfers
Certain transfer-of-control operations
Some operations on the contents of index registers
Certain types of timing functions

Additional hardware can greatly minimize the number of operations of this type required in a program. For example, a set of general registers or a small high-speed control memory can be used to represent multiple accumulators, index registers, and control registers. The availability of such multiple registers will sharply reduce the number of register-to-memory and memory-to-register transfers, the number of index modification operations, and the number of transfer-of-control operations required. There are, of course, many other examples of this type. A somewhat complementary concept is the use of large-capacity low-cost storage coupled with higher speed machine operation to permit the effective utilization of inefficient programs. This increases the size of the program in terms of the number of instructions involved but reduces the man hours required to write a given program by removing the need for polishing and streamlining the program to make it run faster and fit into less storage space.[9]

The operating systems software provided with most computers handles three major functions:

    Input/output control and editing
    Scheduling and storage allocation
    Interrupts and priorities

The operating systems usually represent the most difficult and expensive area of systems programming. It has been estimated that one major computer manufacturer spent $60 million in 1966 for programming PL1, FORTRAN, COBOL, and the operating systems for a family of new computer systems. The operating systems probably represent at least one half of this cost.

[9]Steel, T. B., Jr., "Promising Avenues of Research and Development - Programming Research," Portion of panel discussion at 1965 FJCC.

Many of the functions included in operating systems software can be
implemented by additional hardware. For example, special purpose
control logic and storage hardware can be provided with each type of
input/output equipment to provide a completely standard interface with
the computer so that the programmer and the software system need not
be concerned with the nature or characteristics of the particular
input/output device. Special purpose hardware and buffer storage
can accommodate the differences in characteristics of tape units, disc
files, card readers, keyboards, etc. Small associative memories can
be used to facilitate the cataloging and indexing of data files, the
allocation of storage, and some special functions of particular
importance to naval tactical systems such as track-while-scan and
correlation of multiple target tracks. Hardware can significantly
reduce programming requirements in the servicing of interrupts and
handling of priorities which are very important in real-time systems
such as NTDS.

Most present computer systems use a multi-level storage hierarchy
which usually requires program consideration of the particular level
of storage being used and to some extent the differences in the
characteristics of devices used for different levels. Additional low-
cost logic and special storage techniques can be used to cause this
multi-level storage hierarchy to appear as a single homogeneous
storage to the programmer, thus minimizing the need for programming
attention to the capabilities and characteristics of the different types
of storage. This will be even more important in future naval tactical
systems when one or more types of on-line auxiliary storage are used.
Many of the storage allocation, page turning, and memory protection
schemes used for time-sharing, multi-programming, multi-processor,
and multi-computer systems can be implemented by low-cost hardware
also.

Progress Toward Utilization of Low-Cost Logic and Storage to Reduce Software Costs

Special purpose computers or processors may evolve naturally as multi-computer and multi-processor systems are developed and used on an increasing scale. Hardware features to minimize housekeeping will also tend to evolve as designers find lower and lower cost elements and functions available to them. The hardware implementation of special purpose functions is straight forward, but a catalog of sub-routines in present systems such as NTDS can give a clue to the functions that should be considered for implementation.

Present compilers and higher order languages are a good starting point for considering machine languages and organizations that will simplify programming; but, even with low-cost hardware, further research in programming languages is needed to determine a language closely related to users' problem-oriented languages that is still economically and conceptually feasible to implement as machine language.

Much of the conceptual work necessary to implement operating systems functions has already been done. The large and complex software operating systems that have been developed during the past eight to ten years represent many man years of effort in formalizing the necessary procedures and algorithms. Hence, the starting point should be a study of these operating systems to determine areas that meet three criteria - difficult or unsolved problems, significant numbers of instructions, and procedures and algorithms that are more feasible for mechanization by large-scale integrated circuits or other batch-fabricated hardware. Software functions meeting any of these criteria represent a promising area for development.

Joint hardware, software, and systems design efforts are needed in choosing new hardware/software trade-offs to properly utilize both the results of past work and the capabilities of new technology. In the past, hardware has been traded for software in order to improve speed and performance with the decisions made primarily on a cost-performance basis. In the future, hardware will be traded for software to reduce the cost of programming with decisions made on the basis of total systems cost rather than only equipment costs. Systems designers must consider large-scale integrated-circuit arrays as a new type of device that necessitates major revisions in systems design concepts, machine organization, and hardware/software trade-offs. Navy systems planners should insist on this approach by contractors. The Navy and other military agencies should support research efforts in new machine organizations, solid-state input/output and mass memories, systems approaches that minimize input/output operations, and machine language and programming languages that reduce software costs by greater use of low-cost batch-fabricated hardware.

4. IMPACT OF NEW HARDWARE TECHNOLOGIES ON MAINTAINABILITY

One major phase of this study dealt with the effect of new technologies on tactical military systems and the ways in which these technologies can be utilized to improve maintainability. The term maintainability is used here in the broad sense to include all aspects of field maintenance - repair time and repair costs, parts usage, parts inventory, logistics, test equipment, replacement costs, personnel, training, etc. Training and maintenance personnel (salary, food, and other support costs on station, dependence allowances, etc.) represent the major maintenance costs. Hence, in the maintainability study, major emphasis was placed on factors that reduce the time required for maintenance, the skill level required for the maintenance technician, and the number of maintenance technicians required.

Maintainability considerations alone can justify the development of a new generation of tactical data systems. The improved maintainability and reliability, coupled with reductions in size, weight, and power requirements, which are discussed elsewhere in this report, will necessitate the development of systems utilizing these new technologies regardless of whether performance requirements exist for new systems that justify such development. To achieve these maintainability advantages in future systems, a maintainability concept is recommended which is based on the use of very large functional throw-away units and no shipboard repair, except for electromechanical equipment.

Both the technology and maintainability portions of this study have clearly indicated the need for larger functional throw-away units. High reliability anticipated from batch-fabrication technologies will permit large throw-away units from an economic standpoint. Effective utilization of batch-fabrication technologies will require such large units. Their use will significantly reduce down time, skill levels, and personnel requirements. However,

this improved maintainability in future systems will not occur auto-matically. The fact that these capabilities and improvements will be possible in the early 1970's does not insure that they will be achieved. Adoption of the maintainability concept recommended here and the wil-lingness by the Navy to obsolete and replace present equipment will be necessary to realize the maintainability advantages made possible by new batch-fabrication technologies.

Since this study was primarily concerned with the application of new technologies in 1970 era tactical data systems, emphasis in the main-tainability phase was placed on determining relationships, guide lines, and criteria and on developing concepts for the utilization of these new technologies to achieve improvements in maintainability. The important results of this study lie in the development of conceptual approaches to improved maintainability through the proper use of new technologies. It calls attention to and emphasizes the need for new attitudes and thought patterns with respect to system design, packaging, and maintainability. The effort in this study was directed toward developing criteria for use in determining the cost and functional size of throw-away units, indicating the changes in maintainability concepts and attitudes necessary on the part of Navy personnel (systems planners, budgeters, and users), and providing guidelines for Navy planners in utilizing new technologies to achieve improved maintainability.

Present concepts, approaches, and problems in maintainability were discussed with many Navy personnel, but it was very difficult to obtain quantitative information on present maintenance costs. The effects of new technologies on maintainability were investigated by discussions with technical experts working in each area of new technology and with ones working on maintainability problems, by studying applicable litera-ture, and by evaluation of the information concerning the different

technologies in relation to maintainability problems in future naval
tactical systems.

New technologies providing solid-state electronic and magnetic components
fabricated and interconnected by batch-fabrication techniques offer the
potential for truly significant improvements in reliability and maintaina-
bility. However, reliability and maintainability of electromechanical
peripheral equipment, such as mass memories and input/output equip-
ment, will improve only in an evolutionary manner. The improvements
that can be achieved economically in this type of equipment are limited.
From the maintainability standpoint, the major improvements that can
be achieved with respect to electromechanical peripheral equipment will
be achieved by system approaches that minimize the need for this type of
equipment and by finding solid-state electronic or magnetic replacements
wherever possible. These peripheral equipment questions are considered
in greater detail in the memory, input/output, and display portions of the
hardware technology part of this report (See Section 2 and Appendices
B, C, and D).

The study of maintainability dealt primarily with improvements that can
be obtained in those portions of the system that can utilize solid-state
electronic and magnetic components. It is in the central processor and
internal memory; the solid-state on-line auxiliary storage; and the
digital logic, digital storage, and low level linear and video amplifier
portions of peripheral equipments that truly significant maintainability
improvements can be achieved if new technologies that will be available
by the early 1970's are properly utilized.

Batch-fabrication techniques suitable for the fabrication of central
processors and storage were emphasized in the components and packa-
ging and memory investigations in the hardware technology phase of

this study. Since these fabrication techniques are essential to achieve significant cost reductions and reliability improvements, they were also given major emphasis in the study of maintainability. In general, the higher the degree of batch-fabrication, the lower the cost per function and the higher the reliability - hence, improved maintainability. Lower component costs will permit larger functional throw-away units which in turn will facilitate fault isolation and minimize repair time. Higher reliability will facilitate maintainability by reducing the number of failures and the number of repairs necessary and by permitting a further increase in the size of the throw-away unit. .

New concepts are needed to achieve the maximum improvement in maintainability commensurate with other system requirements such as performance, cost, size and weight, availability, etc. New attitudes and thought patterns are needed in considering equipment design and packaging, repair and inventory costs, and maintenance procedures and techniques. One example is the need for increasing the cost limit for throw-away units (presently in the order of $100) by a factor of several times (possibly over an order of magnitude). Another is the possible elimination of all shipboard repair for certain types of equipments. These changes in attitudes and concepts will be made possible by significant increases in reliability (i. e. reduced mean-time-between-failure) and significant reductions in the cost per element of the hardware involved.

A larger non-repairable unit is required by the functional organization and interconnection and packaging techniques necessary to fully realize the reliability, cost, size, and weight potentials offered by new batch-fabrication technologies. Hence, some of the same changes in attitudes and concepts needed from the maintainability standpoint are also necessary to permit full realization of the advantages of batch-fabrication.

Cost, reliability, and maintainability considerations for batch-fabricated units all favor a large functional throw-away unit, but a difficult problem is raised with respect to flexibility. If functional units are very large, a particular one may be used in only one place in a computer. This creates a problem from both the manufacturing and spares standpoints. If a throw-away unit is a single flipflop, as has been the case in the past, a large number of these can be manufactured and an individual one can be used in any one of a large number of places in the computer. However, if the throw-away unit is a complete parallel adder, only one may be used in the entire computer.

One possible approach that looks attractive is a multi-computer system in which each individual computer is relatively small. This would permit a higher volume of production for each type of unit and would permit the possibility of carrying a spare computer to further facilitate easy and rapid maintenance. It may be desirable to design all types of shipboard systems, including data handling systems, weapons systems, and sensors, to utilize identical small computers with the number of these in each system being tailored to the requirements of the system. If the cost of logical components and storage drop as much as is anticipated, it may be relatively unimportant that one of these standard computers is less efficient in a particular system than a computer designed specifically for that system. Parallel processing systems are another approach that may facilitate the use of large functional throw-away units.

Reliability was considered from both the component and the system level. The effects of different levels of redundancy were considered including:

> No redundancy
> Component level
> Circuit level
> Function level
> Equipment level
> System level

In view of the high reliability anticipated for integrated circuits and batch-fabricated memories, component, circuit, and function level redundancy will not be needed for naval tactical systems. Equipment or system level redundancy is adequate and is preferable because of the ability to use the redundant equipment or system normally for non-critical functions that can be sacrificed when a malfunction occurs.

Packaging techniques influence both maintainability and effective utilization of batch-fabrication techniques. Hence, criteria are needed for selecting the size and configuration of throw-away units and the functional grouping within a throw-away unit. The choice of packaging techniques and functional organization directly influence diagnostic programming, fault isolation, and self test in tactical systems. Functionally large throw-away units only require isolating the fault to a major segment of the computer; hence, self test can be effected by relatively simple diagnostic programs. The cost of discarding rather than repairing these large functional units will be more than offset by savings in the number of maintenance personnel and the training and skill levels required. The savings in maintenance cost are twofold - fewer and relatively unskilled personnel will be required to locate the fault and replace the unit (with the aid of diagnostic programs and self-test hardware) and technicians will not be required for repairing the faulty modules after they are located and identified. Maintenance is achieved by replacement.

4.1 ELEMENTS OF MAINTAINABILITY

In considering the broad question of maintainability several different elements of the maintenance problem should be considered individually. These elements are not all affected in the same way by different approaches to maintainability or by changes in component or packaging technology. A technology change that may be advantageous with respect

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to one element of maintainability may be a disadvantage with respect to another.

The elements of maintainability include:

Maintenance cost	Repair time
Spares inventory costs	Personnel training and skill levels
Logistics or supply costs	Number of maintenance personnel
Replacement part costs	Spares inventory quantity
Repair costs	Personnel availability
Personnel costs	Spares availability
Reliability and failure rate	Spares commonality
Equipment down time	Frequency of spare parts usage
System availability	Test equipment requirements
Fault location time	Diagnostic programming requirements

These elements are all inter-related and, unfortunately, sometimes affect one another adversely. For example, increasing the functional size of a throw-away unit may reduce fault isolation time, maintenance time, down time, and personnel training requirements; but it may, on the other hand, increase the spares inventory cost and reduce the commonality. Hence, in considering the effects of new technologies on maintainability one must be careful not to achieve improvements in some of the elements in maintainability at the expense of excessive costs or severe disadvantages in other elements. Thus, it is necessary to make a careful trade-off analysis when conflicting results are created by a change in maintenance concepts or equipment technology.

Although the effects on different elements of maintainability have been considered at all phases of the study, they are discussed in this report only where a significant advantage or disadvantage exists. This is illustrated in subsequent parts of this section by discussions of the

effects of batch-fabrication and larger throw-away unit packages and the resulting trade-offs that must be evaluated.

4.2 NEW TECHNOLOGIES THAT WILL INFLUENCE MAINTAINABILITY

In the technology sections of this report new technologies are analyzed and evaluated for components and packaging techniques, memories, displays, and input/output equipment. In the investigation of these different areas and individual technologies within each area, improvements in costs and reliability as well as performance were considered.

These new technologies will influence maintainability in two primary ways.

1. Increased reliability and reduced failure rates will reduce the maintenance effort required and will permit increases in the costs of throw-away units. If the failure rate becomes low enough it will reduce the number of technicians required and may eliminate requirements for stocking certain units as spares on shipboard.

2. Lower cost components and the lower costs of batch-fabricated interconnection techniques will permit a significant increase in the functional size of a throw-away unit. This will in turn facilitate fault isolation and reduce the training requirements and the number of maintenance personnel required. At the same time, efficient utilization of batch-fabrication techniques in interconnections and packaging will necessitate larger throw-away units. Hence, the achievement of cost and performance potentials, as well as maintainability improvements, depends upon significantly increasing the size of the throw-away unit. Fortunately, component and interconnection costs, improved reliability, and reduced failure rates will permit such increases in the functional size of a throw-away unit.

The new technologies that will influence maintainability most significantly
are those that are suitable for batch-fabrication, that reduce the cost per
component (or circuit) materially, and that significantly increase relia-
bility. Such technologies that appear both promising and feasible include:

Components and Packaging

Monolithic integrated circuits

Hybrid monolithic/thin-film integrated circuits

Metal-oxide-semiconductor (MOS) integrated circuits

Memories

Integrated circuit arrays

MOS arrays

Planar magnetic thin-film arrays

Plated wire arrays

Etched-permalloy-toroid arrays

Displays

Opto-magnetic displays

Crossed-grid electroluminescent displays with integrated storage

Injection electroluminescence matrix displays

Although not adaptable to batch-fabrication techniques, photochromic dis-
plays, thermoplastic and photoplastic light valves, laser displays, and
solid-state light valves also offer promise for maintainability improve-
ments from the standpoint of both cost and reliability.

Some reliability improvements in electromechanical input/output equip-
ment and mass memories are anticipated, but the major hope for signifi-
cant improvements in maintainability for peripheral equipment lies in
systems approaches that minimize the need for equipment of this type
and in finding replacements for some of the conventional types of
equipments. One example is the replacement of punched paper tapes by
incremental magnetic tapes which will improve maintainability by
increasing reliability (see Appendix D). Another is the use of solid-state

mass memories which will improve the maintainability and reliability of the system by serving as replacements for electromechanical mass memories and for some of the "input/output" functions performed by magnetic tape units in present systems (see Appendix B).

The major improvements in maintainability will occur in the central processor, internal memory, and solid-state on-line auxiliary storage. However, the technologies and batch-fabrication techniques used in central processors and internal memories will also be useful in portions of other equipment where similar functions are required and similar techniques are applicable. This includes the logic, control, and storage functions in display consoles and input/output equipments such as magnetic tape units. By 1970 low-level linear circuits, such as deflection amplifiers and video amplifiers in CRT displays, can be implemented with integrated circuit techniques. High power or high voltage circuits, such as the final stages of the deflection drivers in CRT displays, are more questionable but not completely hopeless within the time frame covered by this study. Communication equipments are not within the scope of this study, but power amplifiers in transmitters will probably represent a problem area.

In computer and data handling systems, the major areas where significant improvements in maintainability do not appear likely are in very large capacity auxiliary storage and input/output equipment. The best approach in these areas from the systems standpoint is to minimize the need for equipments of this type. There is also some question as to whether significant improvements in maintainability can be achieved in the viewing portions (i. e. , the visual transducer) of displays - particularly large-screen displays. However, several potential display technologies, such as opto-magnetic panels and injection electroluminescence matrices, may permit significant improvements in maintainability for console displays, and possibly for large-screen displays.

4.3 EFFECT OF BATCH-FABRICATION ON PACKAGING CONCEPTS AND TECHNIQUES

The importance of batch-fabrication in future systems design has been emphasized in both the maintainability and technology portions of this study. Batch-fabrication is the key to lower costs, higher reliability, and reduced size and weight. However, effective utilization of batch-fabrication technologies will require major changes in packaging concepts and techniques.

4.3.1 Batch-Fabrication and Interconnection Considerations

Eight different levels of packaging and interconnections can be considered in systems using integrated circuits:

1. Packaging and interconnection of the elements of each integrated circuit on a silicon chip.

2. Interconnection between separate circuits fabricated on the same silicon chip.

3. Interconnection between circuits on separate silicon chips that are packaged in the same module.

4. Interconnections between the silicon chips and the external leads of the package.

5. Interconnections between modules on a replaceable unit such as a printed circuit board.

6. Interconnections between replaceable packages in a modular subunit or a small equipment.

7. Interconnections between modular subunits within a unit of equipment.

8. Interconnections between separate pieces of equipment
    in a system.

The first and second level of interconnections are made in the initial
processing of the silicon chip, although they may be made with separate
masks and in separate vacuum deposition operations. To achieve the
potential for improvements in both cost and reliability offered by batch-
fabrication, it is necessary to continually strive to fabricate larger and
larger arrays of interconnected circuits on the same silicon chip.
Hence, emphasis will be placed on increasing interconnections at the
second level and minimizing interconnections at higher levels - particularly
at the fifth, sixth, and seventh levels which represent major factors of
cost and lesser reliability. In fact, it is hoped that eventually a suffi-
ciently large functional throw-away unit can be used that the fifth level
can be completely eliminated and the sixth and seventh levels combined.
In that case, the throw-away unit would consist of large arrays of inte-
grated circuits on a limited number of silicon chips (first and second
levels) that are interconnected by a wiring pattern on a substrate (third
level) which also provides termination points for connecting to the exter-
nal leads of the package (fourth level). Packages of this type would be
either plugged or wired into the equipment containing the interconnections
between the sockets or connectors (sixth and seventh levels). These
equipments would then be interconnected by cables to form the system
(eighth level). Eventually large-scale integrated circuit arrays should
eliminate the third level.

As semiconductor and batch-fabrication techniques advance, the major
limitation on the size of the functional unit (other than cost) will be the
number of external leads that can be provided on a package. Although
packages with larger numbers of leads (in the order of 40 to 100) are
being developed, additional research in machine organization is urgently

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needed to develop functional organizational concepts that will maximize the interconnections within a replaceable package and minimize the interconnections between packages. The way in which the computer is organized into functional modules can greatly increase or decrease the number of connections needed between such modules.

It will be necessary to use different criteria for design efficiency in batch-fabricated systems. In the past, minimizing the number of logical elements has been a major goal of most logical design efforts. In future systems, it will be necessary to utilize logical elements inefficiently in order to minimize the number of interconnections needed between functional modules. For example, frequently in previous computers a given gate or flip-flop has supplied inputs to a number of logical elements in different parts of the machine; while in future systems the logical gate or flip-flop may be duplicated many times in different parts of the system to avoid the necessity for transferring the signal from one module to another. Emphasis must be placed on reducing the number of packages and the number of interconnections between packages - even at the expense of increasing the logical complexity of each package significantly.

From the standpoint of cost and maintainability future systems should use large integrated circuit arrays (either monolithic or MOS) on single chips of silicon with these chips then interconnected by a vacuum deposited thin-film interconnect pattern on a substrate (e. g. the NAFI thin-film circuit techniques). Thin-film resistors and capacitors can be fabricated on the interconnection substrate where high precision or large values are needed. This unit would then become the replaceable or throw-away unit. The marriage of silicon integrated circuit techniques with thin-film fabrication techniques will combine the best advantages of both while maximizing the interconnections that can be

made internally in the package. As the integrated circuit fabrication technology advances, it will become possible to increase the size of the array on a single silicon chip thus minimizing the need for the thin-film interconnection substrate.

The importance of additional research efforts in computer design and machine organization to provide more highly functional organizations that will minimize interconnections between functional modules must be emphasized in order to take advantage of the potential offered by the combination of integrated circuit and thin-film connection technologies.

4. 3. 2 Factors Influencing the Determination of Throw-Away Unit Size
In establishing packaging trade-off criteria it is necessary to consider the effect on the initial cost of the system and on the major elements of maintainability. All of these factors except spares inventory cost, replacement part cost, and spares commonality favor a very large throw-away unit (large in the sense of complexity, not size) with shipboard and field repairs limited to the replacement of these large units. When replaced these units would usually be thrown away, but in certain special cases they might be returned to a state-side depot for repair.

The failure rate and the inventory cost of these large throw-away units will be sufficiently small, relative to present day failure rates and costs, to justify a quite large throw-away unit in preference to smaller ones. Although it is emotionally difficult to accept the idea of throwing away a $2,000 subunit in which only one component has failed, this can be justified if such failures occur infrequently (e. g. less than once per year), and if the use of throw-away units of this size can eliminate the need for one or more technicians on shipboard.

With batch-fabrication technologies the selection of a throw-away unit size involves many inter-related factors, but in general the larger the

throw-away unit size (in terms of complexity) the higher the reliability, the smaller the size, and the lower the cost of the function accomplished by the throw-away unit. Anything that is done in a large functional unit to make components, circuits, or subfunctions within the unit replaceable will tend to decrease the reliability, increase the size, and increase the over-all cost. Although there will undoubtedly be one or more intermediate steps before this is achieved, it is believed that during the 1970's a complete central processor with the capability of a USQ20B will likely become a replaceable unit without repair capability on shipboard, and possibly even a throw-away unit. However, it is too early to predict whether the cost and the mean-time-between-failure will be sufficiently low to permit discarding the unit or whether state-side repair will be required.

The need for a larger throw-away unit can be shown by listing some of the considerations that favor large throw-away units and some that favor small ones.

Considerations favoring large throw-away units:

1. With proper functional organization of the machine, large throw-away units minimize the number of interconnections required from package to package in the system. These interconnections (external to the package) are not as amenable to batch-fabrication as those within the package and hence tend to be more expensive and less reliable. Since batch-fabricated interconnections can be more closely controlled and can be made very cheaply, a larger functional unit tends to improve reliability and reduce cost.

2. Making more of the interconnections within the package permits a smaller size and shorter lead lengths between

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circuits in a given logical function. This tends to reduce power and permit higher speeds - particularly where a large multi-circuit array is fabricated in a single chip with interconnections deposited on the chip.

3. Although large throw-away units may increase the number of different types of spares carried in inventory, they will significantly reduce the total number of items carried in spares. This will reduce logistics requirements.

4. Since packaging costs are a significant part of the cost of completed circuits, the larger the number of circuits in a single package the lower the initial cost. Continuing improvements in integrated circuitry technology will permit larger and larger arrays of circuits to be fabricated and interconnected in a single silicon chip. Interconnection of a number of these chips by printed or deposited wiring on a substrate will permit an even larger interconnected logical function in a single package.

5. Up to a certain point, the limit in putting more circuits in a package is imposed by the number of leads that can be brought out of the package. The ratio of external leads required to the number of circuits in the package is relatively high for smaller package sizes because of the connections that must be made to other packages. However, if the throw-away unit size is increased to the point that complete major logical functions can be contained in a single package, the total number of external connections in the system and the ratio of leads from the package to the number of circuits in the package are significantly reduced. For example, if a

complete binary adder with associated registers is packaged in a single unit, the number of external leads required in relation to the number of circuits in the package would be quite small. A striking example of this is the use of several (e.g. 16 or 32) one word registers interconnected and addressed in a matrix fashion in a single unit compared to the packaging of individual one word registers with external interconnections to each.

6. The larger the throw-away unit the easier it is to isolate faults to a particular unit. For example, if the computer or central processor is a throw-away unit in the extreme case, it would be relatively easy for a technician with minimum training to determine that the fault is in the computer with the aid of a simple diagnostic program. It is progressively more difficult for the maintenance technician to determine that the fault is in the arithmetic unit, in a particular register, in a particular flip-flop circuit, or in a particular diode or transistor on the other extreme. This is very important because it affects the training and skill level required of the technician, the repair time, the number of technicians required, and, perhaps even more important, the down time and availability of the system.

7. Easier fault isolation also reduces the length and complexity of the diagnostic programs required in the computer for automatic fault isolation. A diagnostic program to determine that the fault is in the arithmetic unit is considerably shorter than one required to indicate that the fault is in the third bit position of the adder.

8. Easier fault isolation and minimization of repairs made on shipboard as a result of large throw-away units tend to eliminate the need for special test equipment and check-out equipment. For example, if a throw-away unit is a printed circuit board containing a single flip-flop or a few gates, it is usually necessary to have a board tester capable of determining whether a replaced board is in fact malfunctioning. It should be noted also that this tends to encourage a sloppy form of maintenance which has unfortunate results on maintainability - the indiscriminate replacing of boards until one is found that starts the system working again. Usually, the reliability of a module is reduced after field repair because of the lack of adequate maintenance skills or equipment. If a replaced board is to be repaired on shipboard, the test equipment must be even more complex.

Considerations favoring small throw-away units:

1. The smaller the size of the throw-away unit, the greater the commonality and the ability to utilize one spare unit to replace any one of a large number of units in the system. A printed circuit card containing a single flip-flop is a good example of a small unit with high commonality.

2. The higher commonality for small units may reduce the cost of spares inventory. This is certainly true if the cost per circuit is the same in a large functional unit as in a small one. However, it may not be true if a larger throw-away unit permits a significant reduction in the cost of a circuit (e. g. a flip-flop) compared to the cost of that same circuit as an independent throw-away unit. If a complete computer using large throw-away units costs as much as an equivalent

computer using small throw-away units, the cost of spares inventory required for the one using small units will be considerably less. On the other hand, since batch-fabrication of large throw-away units should significantly reduce the total cost of the computer, the cost of the spares inventory may be less than for an equivalent system utilizing small throw-away units.

3. With manufacturing and fabrication techniques used to date, a small throw-away unit offers manufacturing economies - again due to commonality. A much larger production run of flip-flop boards can be made if the same flip-flop is used in a large number of places in each computer. On the other hand, if each replaceable or throw-away unit in a system is unique, the production volume of each unit would be limited to the number of computers. However, for some of the newer batch fabrication technologies being developed, this may not be a significant factor. This is illustrated by the possibility of making variable interconnect masks under computer control (discretionary wiring).

4. If replaceable units are to be repairable instead of throw-away, the greater standardization permitted by small units facilitates the technician's ability to repair the units.

5. The lower cost of the small throw-away unit is a significant factor if the usage rate is high - i.e., if the reliability is low and the failure rate high. However, the low failure rates anticipated for batch-fabricated circuits minimize the importance of the cost of the unit in relation to other considerations.

6. A small throw-away unit gives greater flexibility in the organization and layout of the logic of the system. Additional research in machine organization for batch-fabricated systems is needed to overcome this disadvantage of large throw-away units.

Large non-repairable throw-away units (large in the sense of function or complexity rather than physical size and cost) containing complete major functional parts of the computer will improve reliability, simplify fault isolation, reduce down time, reduce the number of technicians required and their training and skill levels, permit higher speed operation, reduce logistics and repair costs, and improve the performance and availability of the system. On the negative side, these larger units may increase the number of different types of spares required, the parts cost of replacing a failed unit, and perhaps the total inventory cost. The initial procurement cost of a system using a large throw-away unit will be less if adequate fabrication techniques (e. g. , the fabrication of interconnection masks under computer control) for specialized units are developed.

4.4 THROW-AWAY UNIT COST AND MAINTENANCE PERSONNEL COST TRADE-OFFS IN FUTURE SYSTEMS

In a new procurement initiated in 1965, the next AN/USQ-20B computers purchased will cost approximately $125,000 per computer. By the early 1970's integrated circuit and other batch-fabrication technologies will reduce the cost of computers with equivalent capability to $25,000 or less. This cost reduction will be accompanied by a significant reduction in size and increase in reliability. However, these improvements in cost, size, and reliability cannot be fully realized without changing maintainability concepts and attitudes to permit much larger functional throw-away units. For example, the $25,000 central processor predicted above

might be packaged in 10 to 15 non-repairable units each costing between $1,500 and $3,000.

The reliability of electronics is expected to improve by two orders of magnitude with the rapid development of integrated circuit technologies. Hence, this increase in the cost of the throw-away unit çan be justified on the basis of reduced usage resulting from higher reliability. Logistics costs will be reduced also as a result of reducing the number of items handled through the logistics system. The higher cost of the larger throw-away unit can certainly be justified in terms of fewer technicians required on station and reductions in their required training and skill levels. The elimination of one technician alone will pay in one year for the cost of the complete computer, and hence a complete set of spare units.

On an NTDS ship visited by the study team, it was estimated that 10 of the 33 technicians in the NTDS section were devoted to the maintenance of the computers, their internal memories, and the limited amount of input/output equipment in the system. It is reasonable to believe that reducing the repair task to that of locating and replacing one of ten or fifteen major units comprising the computer will eliminate at least one technician. In fact, assuming that half of these ten technicians are required by the peripheral equipment and half by the computers and internal memories, as many as four of the five technicians concerned with the computers and memories might be eliminated. With very significant reductions in failure rates and fault isolation time and with repairs reduced to merely replacing one of fifteen units, a single technician could easily maintain four computers including the central processors and internal memories.

The predictions and extrapolations from present technology made above may seem far out and perhaps unrealistic. However, based on the

investigations and analyses of this study and lengthy discussions with
integrated circuit, semiconductor, and batch-fabrication memory ex-
perts, these prognostications are believed to be conservative. In the
early 1970's the three USQ20B computers and their internal memories,
two magnetic tape units (four tape transports), punched paper tape
reader, teletype printer and punch, and several large banks of
mechanical interconnection switches in a typical NTDS installation
can be replaced with three small batch-fabricated computers and in-
ternal memories including internal electronic switching and gating, a
large capacity solid-state random access mass memory, one magnetic
tape unit (two tape transports), and a keyboard-printer unit with an
associated incremental magnetic tape recorder. The keyboard printer
unit may be a non-mechanical keyboard and non-impact printer with no
moving parts except for paper feed. At the most, three maintenance
technicians would be required for this complete computer system com-
pared to approximately ten at present. The savings from elimination of
seven technicians would exceed the cost of the computer system in two
years.

From the maintenance standpoint, the NTDS system on the ship visited
by the study team was divided into three major areas - the computer
system, the display/input consoles, and the communications terminals.
The discussion above has dealt exclusively with the computer system
where the greatest gains in maintainability can be achieved through the
use of new technologies. However, the same considerations and reason-
ings apply to portions of the display/input consoles and the communications
terminals. For example, the analyses presented above are equally appli-
cable to the digital control logic and storage in the display/input consoles.
Hence, the proper utilization of new technologies will permit maintaina-
bility improvements in these other two areas also but to a lesser extent
than in the computer system since major portions of the equipments in

these areas are not as readily amenable to batch-fabrication technologies in the near future.

It is important to point out that these discussions of improved maintainability are valid only if we assume the design of a new generation system utilizing these new technologies. The fact that these capabilities and improvements will be possible in the early 1970's does not assure that they will be achieved. This depends on factors such as the willingness to obsolete and replace present equipment and the willingness of Navy systems planners, budgeters, and users to adopt the radically different attitudes toward maintenance procedures and costs called for by the maintainability concept advocated here. This maintainability concept is based on very large functional throw-away units and no shipboard repair, except for any electromechanical equipment that may still be necessary.

5. IMPACT OF NEW HARDWARE TECHNOLOGIES ON FUTURE NAVAL TACTICAL SYSTEMS

Any new tactical system developed in the future will undoubtedly represent increased scope and increased performance requirements. However, improvements in maintainability and reliability and reductions in size, weight, and power that can be achieved by the use of new technologies will be so great that they will justify the development of a new system -- even if there were no requirements for increased performance or broader scope. Significant savings in space and weight will be of particular importance on smaller ships. This study did not include a cost effectiveness analysis, but it is believed that increased system effectiveness resulting from increased availability coupled with reductions in personnel training levels, the number of maintenance personnel required on shipboard, lower equipment costs, and lower logistics costs will justify the cost of developing a new system.

Maintenance personnel savings were discussed in Section 4.4. To illustrate the savings in size, weight, and power requirements that will be possible with technological advances anticipated by 1970, each equipment in the present NTDS system (excluding communications) has been compared with estimates for equipment capable of providing the same performance but utilizing new technologies. These comparisons, shown in Table 5-1, also serve to illustrate the types of equipment in which significant improvements are anticipated and those in which only minor advances are expected. The estimates for future equipment include size and weight reductions in cabinets and cabling made possible by the size and density of batch-fabricated circuits and interconnections. The estimates for equipment in 1970 are believed to be

Equipment	No. in System	Present NTDS			Equivalent 1970 System			Total Reduction (No. X Difference)		
		Size Cu. Ft.	Weight Lbs.	Power Watts	Size Cu. Ft.	Weight Lbs.	Power Watts	Size Cu. Ft.	Weight Lbs.	Power Watts
AN/USQ20B Computer	3	51	2400	4500*	3	150	250	144	6750	6900
Magnetic Tape Unit	2	46	1400	2700	30	950	2100	32	900	1200
Video Processor	2	46	1500	2100	4	200	400	84	2600	3400
Teletype & Adaptor	1	29	300	500	20	200	350	9	100	150
Paper Tape Unit	1	15	260	700	10	170	470	5	90	230
System Monitor Panel	1	14	400	240	7	200	150	7	200	90
Terminal Equip. Logic	1	32	1000	1400	3	100	200	29	900	1200
Keyset Central	1	32	960	1400	5	160	200	27	800	1200
Keyset Universal	8	3	100	200	2	70	120	8	240	640
MG Set	3	14	1000	1000**	5	300	150	27	2100	2550**
MG Control	3	11	320	----**	2	120	----**	27	600	----**
Interconnection Panel	8	14	250	----	0.5	20	---	108	1840	----
Central Pulse Amp	1	27	630	390	12	300	200	15	330	190
Symbol Generator	1	32	700	680	4	150	150	28	550	530
Display Console	12	32	1200	1400	16	500	600	192	8400	9600
Totals for Typical Systems		1113	38410	49810	371	12010	16080	742	26400	33730

*Includes 2000 Watts required to run the blowers
**Power input to MG Set and MG Controller in excess of that delivered to the computer

COMPARISON OF EQUIPMENTS OF TYPICAL NTDS SYSTEM
WITH EQUIVALENT PERFORMANCE EQUIPMENTS FEASIBLE IN 1970
Table 5-1

conservative for the digital electronic equipment but may be somewhat optimistic for some of the electromechanical peripheral equipment.

These comparisons indicate that significant advantages can accrue to the Navy in utilizing new technologies even without considering increased performance requirements. For a typical NTDS installation, the estimates for equipment feasible in 1970 represent reductions of approximately 67% in volume, weight, and power requirements. In addition to 'he advantages illustrated by these comparisons, improved maintainability and reliability improvements of greater than one order of magnitude for digital electronic equipments provide strong arguments for the utilization of these new technologies at the earliest possible time. Analyses presented in Section 4. 4 indicate savings of 7 maintenance technicians on a typical large ship. The maintainability improvements will be reflected not only in reduced numbers of maintenance technicians required on shipboard but also in reduced training required for maintenance personnel, reduced supply and logistics requirements for spare parts, and reduced down-time and increased availability.

Technology advances will permit prototype equipments with these characteristics in 1970, but the actual availability of such equipment will depend upon the funding of the development of such equipment and when system design is started. Operational systems for the fleet will, of course, lag the prototypes by one to three years. Hence, achieving in the early 1970's the improvements in performance, maintainability, reliability, size, weight, and power made possible by new hardware technologies require starting systems analysis and design immediately and prototype hardware design within one year. Otherwise, the Navy will not realize the significant advantages of batch-fabrication technologies until several years after they are technological and

economically feasible. Such a delay would represent not only a loss in capability, but also a significant dollar loss in maintenance, personnel, and space costs.

It should be noted, however, that some of these advantages can be achieved in the interim in an evolutionary manner without waiting for a completely new system design. For example, new display consoles, computers, or interconnection panels could be introduced into the present NTDS system. The Navy is presently investigating some such equipment replacements including tape units, interconnection panels, and repackaging of several I/O devices into a single cabinet.

Appendix A

COMPONENT AND PACKAGING TECHNOLOGY

1. GENERAL

Although many other types of components have been proposed and investigated, semiconductor devices continue to occupy a dominant position in the implementation of both digital logic functions and linear circuits in digital computers and peripheral equipments. This will continue to be the case, including applications in future Naval tactical systems, for the foreseeable future. However, discrete component semiconductor circuits have given away to integrated circuits with a limited number of components or gates per chip. These in turn are giving away to large scale integrated circuits (LSI). It is anticipated that by the early 1970!s the logic and control portions of many digital computers and peripheral equipments will be implemented with LSI -- large arrays of integrated circuits with hundreds or thousands of gates or other types of circuits interconnected on a single silicon chip. This will certainly be true for the computer portions of future naval tactical systems and probably for the digital logic and control functions in most peripheral equipments,including displays.

Batch fabrication is the key consideration for future computer systems since this will permit smaller size and weight, lower cost, higher reliability, and improved "throw-away" maintenance. Batch fabrication techniques will be important in the fabrication of the interconnections between circuits as well as the components and circuits themselves. Silicon semiconductor circuits are ideally suited to batch-fabrication techniques and several different approaches to the fabrication and inter - connection of large arrays of logic and storage circuits are being developed.

Both bipolar monolithic circuits and metal-oxide-semiconductor (MOS) circuits will be used, but there is appreciable controversy at this time as to which technology will play the greater role in future digital systems. Bipolar monolithic integrated circuits are faster, but MOS devices are believed easier to fabricate in very large repetitive arrays. Hence, MOS devices may be used in applications where high speed is not r equired and in applications where very large standardized arrays can be used -- e. g., large memory arrays.

During the past two years interest in thin-film and hybrid circuits have decreased because of the rapid advances in monolithic integrated circuits and MOS arrays. However, the use of thin-film techniques for fabricating innerconnections on a passive substrate to which large integrated circuit arrays can be connected is still attractive. Thin-film techniques continue to be attractive also for fabricating high valued or high tolerance resistors and capacitors for linear circuits-- particularly where these components are deposited with thin-film techniques on the silicon chip into which the monolithic integrated circuits have been diffused.

This appendix will discuss technical developments in components and packaging techniques with particular emphasis on integrated circuits because of their dominance in this field Other component technologies are also discussed briefly and the reasons for their failure to overtake semiconductor devices are indicated. The effect of the se circuit and packaging technologies on naval tactical systems in the 1970-80 era are considered. Most of the component anc packaging technologies discussed here were previously covered in the material prepared in 1964 for the ANTACCS final report, but this appendix reflects the results of the continuing research and development in these technologies during

the past two years. During this period some of the other types of component technologies have fallen even farther behind, and developments in large-scale integrated circuits arrays and other batch-fabrication technologies anticipated in that report have been confirmed. In many respects the progress in large-scale integrated arrays has been much faster than anticipated so that capabilities discussed as possibilities in 1964 and 1965 can now be considered actualities.

Batch-fabrication techniques are important from the standpoint of lowering the costs of the basic circuits, but they are perhaps even more important from the overall systems standpoint in permitting many circuits to be innerconnected with higher reliability and lower costs in a much smaller physical space. These latter advantages permit lower production costs and hence lower equipment costs to the Navy. They may be even more important in making possible significantly different maintainability concepts and approaches. The high reliability (long MTBF) and low initial cost of large integrated circuit arrays will permit much wider use of replacement and "throw-away" maintenance techniques. It is believed that shipboard repair of the digital logic and control portions of the computer system can be essentially eliminated. When a failure occurs relatively simple diagnostic programming techniques can isolate the failure to a particular large modular unit which can then be replaced by the technician with a spare. In most cases, the failure rate and cost will be sufficiently low to permit throwing the failed module away, but in other cases it may be desirable to return the unit to a shore maintenance depot for repair. However, full achievement of the maintainability advantages offered by batch-fabrication techniques for future naval tactical systems depends upon willingness to accept a higher cost for throw-away units. This approach, which can be justified by the longer

time between failures, is essential because attempting to break the
system into smaller modules to hold down the cost of the throw-away
unit unfortunately results in a significant increase in the interconnections
external to the package or silicon chip and, hence, in reduced reliability
and increased costs.

Semiconductor and thin-film component fabrication techniques are
closely related to and interrelated with packaging concepts and tech-
niques. Some of the fabrication techniques for making interconnections
between components and circuits on a silicon chip are directly appli-
cable to the fabrication of interconnection patterns on a substrate for
making connections between silicon chips. Since the selection of
specific types of components imposes unique requirements on pack-
aging techniques, the method of packaging arrays of components cannot
be considered independently of the nature of the component itself. For
example, the development of large-scale integrated circuit arrays with
hundreds or thousands of circuits on a single silicon chip significantly
reduces the number of interconnections that must be fabricated external
to the chip on a substrate or by means of a printed circuit board. On
the other hand, the number of leads that can be connected to a single
silicon chip will seriously limit the number of circuits that can be con-
tained on the chip unless machine organization techniques can be developed
that will permit the chip to be selfcontained to a large extent with a high
degree of interconnections on the chip itself. In other words, the logi-
cal organization of the machine must permit a high ratio of internal to
external interconnections for each package or module. The use of large
interconnected arrays of circuits will eliminate some of the levels of
interconnections found in present systems. This will further contribute
to improved reliability and lower costs as well as reduced size and weight.

Major emphasis must be placed on machine organization (architecture),

system design, and maintainability concepts that permit the fabrication of as many logic circuits as possible in a single package that can be considered a replaceable, and preferably a throw-away, unit. The consequent reduction in interconnections, wiring, and connectors will be of significant importance since the increased reliability offered by integrated circuits will tend to make connectors and wiring the major sources of failures.

2. TYPES OF COMPONENTS

There are many specialized and secondary uses of circuits and component
techniques in tactical data systems, but the discussions in this appendix
are concerned primarily with those used for implementing logical
functions in mechanizing the control, arithmetic and processing portions
of the system. Hence, consideration will be limited to digital components
and circuit techniques. Special digital components, linear circuits,
and high-power or high-voltage circuits, such as memory electronics,
cathode-ray-tube circuitry and displays, and circuitry for interfacing
with electro/mechanical components, will not be considered here. They
are considered as part of the memory system, the display system, or the
input/out equipment.

Many different technologies have been proposed and investigated for
implementing digital logical functions including magnetics, optics,
cryogenics, fluidics, and electronics. However, none of the others have
been able to compete successfully with electronic techniques for general
purpose applications although some have advantages in special cases.

2.1 Magnetics

All-magnetic logic has been considered for many years and computers
have been designed in the past in which the active components were
magnetic amplifiers. [1,2,3,4,5,6] However, the widespread use of
magnetics continues to be restricted to storage applications. At one
time it was believed that all magnetic logic would provide higher reli-
ability than electronic circuitry, but recent advances in integrated circuits
have dissipated that advantage. High radiation resistance, high tempera-
ture tolerance, and low power in standby conditions or at low frequencies
are major advantages for certain types of aerospace applications, but
are not of major importance in naval tactical systems. The major

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disadvantages of all magnetic logic have been the inherent slow speed, the lack of a steady-state output indications, and the difficulty of batch fabrication.

One of the more attractive applications of magnetics, other than conventional memories, is in the implementation of shift registers.[7] However, for small size shift registers, MOS integrated circuits are already sufficiently attractive to make the widespread use of magnetic shift registers questionable in the future except for adverse environment applications. However, some recent developments in the fabrication of thin-film all-magnetic logic networks offer promise for batch fabrication of magnetic logic.[8] This may make magnetic logic more attractive for certain special applications in the future, but it is doubtful that it will be able to compete successfully with semiconductor integrated circuits for the major logical functions in future naval tactical systems.

2.2 Optics

Optical components offer attractive possibilities for future computers because of the speed that is theoretically possible.[9,10,11,12,13] Fiber optics, lasers, and injection-electroluminescent semiconductors provide properties that may be useful in future computers, but their application appears to be limited to special functions for the foreseeable future.[14,15,16,17,18] No developments in optics have been sufficient to justify an expectation that optical logic will be used in a major way before 1975. Optical components and techniques are currently in widespread use in displays and will likely be used in memories, but their use as logical components is questionable for the foreseeable future. However, optical techniques may be used for some special functions within the logical portions of future systems. One example of this is the use of optical paths for making interconnections where the use of physical connectors for electrical signals would be difficult.[19]

As stated by Mr. W. V. Smith at the ONR Symposium on Optical and Electro-Optical Information Processing on November 10, 1964, "... (in conventional computers) neither the results presented at this conference nor my independent consideration of the physics involved, suggest obvious simple reasons why light is advantageous."[20] However, there are some types of "non-conventional" data processing applications for which optical techniques are well suited. These include image processing, pattern recognition, and adaptive systems.[21, 22, 23, 24, 25]

2.3 Cryogenics

It appears increasingly unlikely that cryogenic techniques will offer sufficient advantages to justify their use in logical components. Cryogenics have failed to achieve the potential claimed for them for over ten years. Some work is still underway on cryogenic techniques for memory applications, particularly associative and large-capacity memories, but these efforts are decreasing. Even the proponements of cryogenics have admitted that logical components are the least likely application for cryogenic techniques in computer systems.[26, 27]

2.4 Fluidics

Fluid logic is very slow compared to the other types of components discussed here, but, it offers some advantages where it is necessary to interface with electro-mechanical equipment or with human operations since the speed of these functions are limited.[28, 29, 30, 31, 32] Fluid components have been proposed for applications such as keyboards, desk calculators, and control functions. They are particularly advantageous in adverse environment applications where high radiation fields and high temperatures may be encountered. Fluid logic is attractive in some input/output devices where fluid logic elements can be coupled directly to fluid control elements, thus eliminating the necessity for transducing from one type of device to another. Fluid logic fabrication techniques that are amenable to batch fabrication have been demonstrated in the form of injection molding techniques. Although

fluid logic may be applicable for some shipboard functions, such as control systems applications, it will not be competitive with semi-conductor integrated circuits for implementing logical functions in the computer and digital portions of future naval tactical systems.

2. 5 Electronics

Electronics will continue the dominant role as logic and control elements in computer systems that they have held for almost 20 years. Relays and vacuum tubes were displaced by discrete component semiconductor circuits which in turn have given way to integrated circuits during the past two years. For the majority of logical functions in future computers present types of integrated circuits having a limited number of circuits on a single silicon chip will give way to large integrated circuit arrays (LSI), if machine organization techniques can be developed to effectively utilize very large arrays or if effective customizing techniques (e. g. discretionary wiring) are successfully developed. , The characteristics anticipated for different types of integrated circuits are shown in Table A-1.

TECHNOLOGY	PROPOGATION DELAY	SYSTEM CLOCK RATE
Hybrid semiconductor/ thin/film circuits	1 to 10 ns	5 to 20 mc
Monolithic circuits	0. 5 to 10 ns	10 to 50 mc
Metal-oxide semi-conductor (MOS) circuits	20 to 100 ns	2 to 10 mc
Silicon-on-sapphire (SOS) circuits	20 to 100 ns	2 to 10 mc
Active thin-film circuits	will not be available by 1970	

INTEGRATED CIRCUIT CHARACTERISTICS ANTICIPATED BY 1970

TABLE A - 1

Hybrid thin-film/discrete circuits with thin-film passive components and discrete semiconductor active components were of considerable interest in 1964, [33,34]. However, these are being supplanted by monolithic integrated circuits for most digital functions in military systems. Compatible hybrid circuits in which thin-film resistors and capacitors are deposited on the surface of a monolithic silicon circuit are still attractive for analog circuits where large value or high tolerance resistors or capacitors are required. [35,36]. Thin-film fabrication techniques will continue to be important for interconnections, both for interconnecting elements and circuits on a single silicon chip as well as providing interconnection patterns on a passive substrate by means of which several large chips can be interconnected.

Interest in active thin-film circuits seems to have waned during the past two years--probably as a result of the rapid progress in monolithic and MOS integrated circuits. Active thin-film circuits in which active components as well as passive components are fabricated by thin-film techniques potentially offer a cheaper and easier method of fabricating large arrays, but practical feasibility for this type of circuit has yet to be proven. [37,38,39]. These may be useful for naval tactical systems in the 1975-80 era, but it is very unlikely that they will be competitive with monolithic bipolar or MOS integrated circuit techniques prior to that time.

Monolithic bipolar integrated circuits and metal-oxide-semiconductor (MOS) circuits have both been proven feasible and are in use in military and commercial computers at present. [40,41,42,43]. These two types of circuits will almost certainly dominate logic and control circuits and will play an important role in high-speed control and

scratch pad memories through 1975 and possibly through the entire 1970-80 period. The outlook for MOS circuits has improved significantly since 1964. There is considerable controversy within the semiconductor and computer industries at present as to which of these two types of semiconductor technologies will be the more important. [44,45] Monolithic integrated circuits have a decided advantage in speed while MOS circuits offer lower power consumption, higher component density and, the possibility of easier fabrication of very large arrays. However, it is questionable whether the fabrication simplicity will be sufficient to overcome the speed advantages of bipolar circuits. Lower power consumption will be a decided advantage for MOS circuits in applications, such as spaceborne systems, where power consumption is a primary consideration, but power will not be a deciding factor in most shipboard and ground-based application.

The high yield necessary to successfully fabricate large arrays of circuits may be more feasible with MOS circuits because of the smaller number of processing steps required, but it is not clear at this point that the number of steps will be the dominant factor in processing arrays. [46] In monolithic bipolar circuits it is necessary to control the thickness in the diffusion layer in the semiconductor while in MOS circuits it is necessary to control the thickness of the oxide layer. Hence, process control problems are transferred from the body of the semiconductor to the surface. Many feel that surface effects will be more difficult to control, but significant progress has been made in this direction.

Because of the higher circuit complexity that can be achieved per unit of chip area, it is likely that MOS devices will be used in future systems where speed is not important. However, in most computer applications higher circuit speeds result in higher system performance; hence, bipolar monolithic circuits will probably be used in most applications. Exceptions will be those cases where the required circuit speed is limited by external factors such as interfaces with electromechanical equipment or manual operations.

Silicon-on-saphire (SOS) circuits are fabricated by growing a layer of silicon on a passive saphire substrate and then etching away unwanted silicon to provide complete isolation between devices. [47,48,49.] Although the fabrication techniques are different, the characteristics of silicon-on-saphire circuits are very similar to those of MOS circuits. Hence, silicon-on-saphire circuits will be considered in the same category as MOS circuits in the remainder of the discussions in this appendix.

2.6 Comparison of Component Technologies

The advantages and disadvantages of each of the component technologies discussed earlier in this section are summarized in Table A-2. Since monolithic bipolar and metal-oxide-semiconductor integrated circuits will be the dominant component technologies for the next five to ten years, the majority of the discussions in the remainder of this appendix will be devoted to these two types of integrated circuits. Particular emphasis will be placed on their use in large scale-integrated circuit arrays (LSI).

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	ADVANTAGES	DISADVANTAGES	COMMENTS
Magnetics	High reliability; Radiation resistance; High-temperature operation; Low stand-by power.	Slow speed; No steady output indication; Logical circuits more complex and multiphase clock usually required	Not competitive with semi-conductor integrated circuits for computer applications except perhaps in peripheral equipments. May be applicable to weapon direction and ships control systems.
Optics	High frequencies possible; Fiber optics can conduct light around curved path; High density possible; Can provide complete isolation from electrical circuits.	Feasibility for logical elements is farther in the future; Digital technology and fabrication techniques not well developed.	Of major importance in displays; Will be used in memories. Use as logic components in systems will probably not occur before 1975.
Cryogenics	Low cost in large quantities.	High "overhead" costs; Present approaches to logic are relatively slow.	Feasibility and availability questionable; Shipboard or groundbased use doubtful.
Fluidics	Less affected by temperature, electromagnetic fields, and nuclear radiation; Easy mechanical and manual inter-face; Perhaps low cost in batch-fabricated form; High reliability and long shelf life.	Very slow; Size and weight large relative to semiconductor integrated circuits; Unsatis-factory cost/speed ratio for most applications.	May be applicable to some ship-board functions such as weapon direction and ships control; Not competitive with integrated cir-cuits for most tactical data systems applications.

COMPARISON OF COMPONENT TECHNOLOGIES FOR 1970
TABLE A-2

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ADVANTAGES	DISADVANTAGES	COMMENTS
Hybrid Discrete/Thin-Film Integrated Circuits		
Inherent isolation; High precision and large value resistors and capacitors easier to obtain; Low temperature coefficient; Versatility flexibility; and lower tooling costs for small runs.	Expensive active elements; Ultimate reliability poorer than monolithic integrated circuits; Higher cost in large volume.	Useful for analog or linear circuits and where a high ratio of passive to active components is required, but being replaced by "compatible" monolithic/thin-film techniques.
Monolithic Integrated Circuits		
Low cost; High speed; High reliability. Large arrays of circuits can be batch fabricated on a single silicon chip. Less sensitive to surface effects than MOS.	Passive components have poor tolerances, and take up too much space on the chip; Difficult to fabricate large capacitors.	Isolation techniques have been improved; Expected to be the major type of circuit used to mechanize logic functions in computers of the 1970 era.
Hybrid Monolithic/Thin-Film (Compatible) Integrated Circuits		
Combines some of the advantages of Hybrid Discrete/Thin-Film with some of the advantages of Monolithic techniques; Can be used in linear or high frequency circuits where isolation, good tolerances or large value R and C are required	More expensive than Monolithic for digital logic circuits;	Expected to be used in 1970 era systems to supplement Monolithic circuits where required characteristics can be obtained more easily-- particularly for analog circuits.

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TABLE A - 2 (continued)

Metal-Oxide-Semiconductor (MOS) Integrated Circuits

Fewer processing steps; Inherently isolated; Larger arrays are feasible at present. Low noise; Low power; Higher component density.

Active Thin-Film Integrated Circuits

May be very cheap ultimately; Substrate size not limited to size of a single silicon chip; Inherent isolation Fabrication of very large arrays will be possible when technology becomes feasible.

DISADVANTAGES

Surface effects more difficult to control; Slow speed; Not as well suited to linear or analog circuits.

Only FET types look promising and they will be slow; Difficult to make reproducibly at present; Stability problems; Feasibility and availability questionable.

COMMENTS

High impedance levels are an advantage for some applications and a disadvantage for others. Very attractive for large arrays, such as storage arrays, and for low power applications.

TABLE A - 2 (continued)

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3. FUNCTIONAL USES AND TYPES OF LOGICAL COMPONENTS

Many different functional uses will exist for logical components in future naval tactical systems. The type of logical components used, the characteristics required, the cost performance trade-offs, and the packaging and interconnection considerations will depend upon the over-all system characteristics and the specific function for which the circuit is used. The following list illustrates the functional uses of logical circuitry that may be required in a 1970 naval tactical system.

In Central Processors

1) Internal control logic

2) Input/Output control and synchronizing logic

3) Arithmetic logic

4) Timing and synchronizing circuitry

5) Memory selection and addressing logic

In Peripheral and Auxiliary Equipments

1) Control and synchronizing logic

2) Selection and addressing logic

3) Timing and sequencing circuitry

4) Electro-mechanical interface circuitry

5) Communications control and driving circuitry

A single type of circuitry can conceivably serve most of these functional uses, but it is unlikely that a single type of circuitry will be optimum for all of these functions. For example, the internal control logic in the central processor will require higher speed circuitry than will the control functions in the peripheral equipments. The fact that the arithmetic logic tends to be highly repetitive, while the control logic tends to be more unique and non-repetitive, has important implications on the type of integrated circuitry used and, particularly, on the packaging and interconnections for these circuits. For example, it is possible to package an entire shift register or several stages of a parallel adder in a single module due to the

repetitive nature of these circuits. On the other hand, most of the control logic is unique rather than repetitive in conventional computer organizations; hence, fewer logical functions can be packaged in a single module without adversely affecting the flexibility of the module and the frequency of its usage.

In some cases, the type of logical circuitry used may be dependent upon the choice or selection of components or devices for other functions. For example, the choice of a particular type of memory will certainly affect the choice of memory selection and addressing logic circuits. The same is true for the logical circuitry for buffering and synchronizing input/output equipment. The need for interfacing with electromechanical equipment or human operations places different speed and power requirements on the logical components used for those applications.

The use of at least two different sets of logic circuits with significantly different operating speeds may be justified. Most of the internal logic of the machine should be mechanized by high-speed logic circuits while circuits with an order of magnitude less speed capability will be adequate for most of the peripheral equipment. The slower circuits may also be used in the central processor for input/output control and buffering functions. The trade-off between the cost saving for the lower speed circuits and the increased maintenance and logistics problems imposed by having two different sets of circuits should be analyzed in deciding whether different types of circuits should be used. For Navy shipboard applications, spares and logistics considerations may easily override questions of component cost and lead to a decision in favor of a single set of circuit types.

Requirements for components and packaging technology in a 1970 shipboard tactical data system will exist in the central processor, the displays, and the auxiliary and peripheral equipments. The component

and packaging requirements associated with the memory are discussed under memory technology in Appendix B. Aside from the memory electronics, all of the requirements for components and packaging technologies within the central processor will favor relatively low-power and high-speed logic circuits that can be implemented easily with integrated circuit technology. In addition to logic circuits, the displays and peripheral equipments will require some relatively low-voltage, low-power linear circuits that can be mechanized by integrated circuit technology similar to that used in the central processor. However, in the displays and peripheral equipments, requirements will exist also for linear integrated circuits providing either high precision, high-power, or high-voltage. High precision linear circuits will be required in analog-to-digital and digital-to-analog conversion equipment and in display equipments; high-power circuits will be required in the control of electromechanical equipment and in some types of displays; high-voltage circuits will be required in cathode ray tube consoles and possibly other types of displays. High precision is difficult, high-power very difficult, and high voltage all but impossible with present integrated circuit technology.

For the logical components in the central processor and peripheral equipments, no requirement is anticipated for either high-power or extremely high speeds. Power dissipation should not exceed 25 milli-watts per gate. Propagation delays in the order of 20 nanoseconds per gate and system clock rates in the order of 5 to 10 megacycles should be adequate. However, to a very large extent, the basic circuit speeds required are a function of the machine organization and logical design techniques used. For example, much higher basic speeds will be required for a serial computer than for a parallel computer for equivalent system performance. The estimated requirements cited above are based on the assumption of a machine organization in which all of the bits of a word are transferred or operated upon in

parallel. Highly parallel systems in which multiple arithmetic or processing operations take place in parallel could use slower circuits for a given system performance than a conventional computer organization.

A final evaluation and selection of components and packaging techniques should be made in close cooperation with the study and evaluation of machine organization and system design approaches since each is dependent upon the other.

In considering integrated circuits for logical components, it is also necessary to consider the type of logical configuration to be used. The major types are:

> Direct coupled transistor logic (DCTL)
>
> Resistor transistor logic (RTL)
>
> Diode transistor logic (DTL)
>
> Low Level Logic (LLL)
>
> Resistor capacitor transistor logic (RCTL)
>
> Transistor coupled transistor logic (TTL)
>
> Emitter coupled transistor logic (ECTL) also referred to as current mode logic (CML or MECL).

The choice between these different types of logical circuit depends upon the function for which the circuit is chosen and the method of fabrication of the integrated circuit itself. The relative importance of speed, cost, power, size, and reliability will vary with different applications and different circuit fabrication techniques. The major advantages and disadvantages of each type are shown below: [46,50,51,52,53,54]

Logic Circuits	Advantages	Disadvantages
DCTL (Modified)	Low-power; Simplicity; Easily integrated; Inexpensive..	Noise sensitivity; Low fan-out
RTL	Simplicity; Better load.	Noise sensitivity; Slower speed than DCTL; Resistors require large area in integrated circuits

Logic Circuits	Advantages	Disadvantages
DTL	Good noise immunity; Good fan-in; Good fan-out; Low power	Slower speed; Some large resistors required; Two power supplies required.
RCTL	Good load distribution; Good noise rejection; High fan-out; Low-power.	Slower speed; More complex circuit.
TTL	High speed; Low power; Easily integrated.	Moderate fan-out; Limited fan-in; Cannot connect collectors to make logical "or".
LLL	Good noise immunity; Relatively good fan-out; Low power	Moderate speed; One large resistor.
CML	Highest speed; Simplicity; Good load distribution; Small resistors.	More critical circuit parameters. High-power; Two power supplies; Noise sensitivity; Temperature sensitive.

There are several other types of logic circuits that represent variations or modifications of one or more of those above to achieve improvements in a particular characteristic, frequently at the expense of another. Some integrated circuit families or arrays use more than one type of logic circuit -- e. g. compatible TTL and DTL circuits may be used together to better match the speed, power, and fan-in, and fan-out requirements of specific logical functions. The advent of integrated circuits has changed the criteria for selecting logic circuit types because of the shift in relative cost of active and passive components. For example, RTL using only one transistor and several resistors was very cheap relative to other types for discrete circuits, but is less desirable for monolithic integrated circuits because of the silicon area required to fabricate the resistors. DCTL, TTL, and CML circuits, on the other hand, consist primarily of active elements (diodes or transistors) and are relatively easy to fabricate with integrated circuit techniques.

4. INTEGRATED CIRCUITS

In 1964 it was estimated that integrated circuits would account for approximately 50% of all military electronics in 1970, and 75% in 1973. [55,56,57] Since digital circuitry is more adaptable to integrated circuit techniques, it was estimated that approximately 70% of the electronics in computers and data processing equipment will consist of integrated circuits by 1970 and that the figure would be closer to 90% for the logic portions of new digital equipment by 1970. Rapid advances in integrated circuit technology during the past two years make these estimates seem conservative. The dominance of integrated circuits in future military systems has been underscored by Department of Defense personnel and policies. [58,59] For new military equipment becoming operation in 1970 or later, essentially all of the digital logic circuits and most of the other circuits in computers and data processing equipment will utilize integrated circuit techniques. The major exceptions will be those circuits requiring high voltage or high power for interfacing with cathode ray tubes or electro-mechanical devices in displays and other input/output equipments.

Batch-fabrication of large numbers of elements in a single set of processing operations is the key to smaller size and weight, lower cost, higher reliability and improved maintainability for future naval tactical systems. Integrated circuit fabrication is the most highly developed batch-fabrication technique at present and the one on which the greatest research and development efforts are being expended. Silicon semiconductor integrated circuits are ideally suited to batch-fabrication techniques both for the devices themselves and for the interconnection of many devices into a large array of logic or storage. [60,61] The majority of the electronics in future systems will be fabricated

with either monolithic bipolar or MOS integrated circuits. The choice between these two will depend upon the importance of speed in a particular application and upon whether MOS techniques ultimately prove sufficiently cheaper and easier to fabricate in large arrays than bipolar circuits to justify their speed limitations. Estimates for MOS circuits range between 10 and 50% of the total integrated circuit market within five years. [44,45]

Monolithic bipolar and MOS circuits are discussed in greater detail in this section since these are the two technologies most appropriate and promising for implementing logical functions in future Naval tactical systems.

4.1 Monolithic Bipolar Integrated Circuits

This type of circuit is completely integrated. [46] Active elements (e. g. , transistors and diodes) and the associated passive elements (e. g. , resistors and capacitors) necessary to perform a specific circuit function or set of circuit functions, are fabricated by a series of diffusion processes in a single silicon chip. Interconnections are fabricated by vacuum deposition processes on top of the diffused components. This circuit has the advantage that all components in the circuit are made during the same series of operations, and that multiple circuits can be batch-fabricated in a single set of operations. This type of circuit should ultimately be cheaper to fabricate and more reliable due to the ability to make all interconnections by vacuum deposition processes. It is adaptable to the batch-fabrication of large interconnected arrays such as a complete arithmetic unit. There have been three major problems with respect to monolithic integrated circuits to date:

a) The interaction between semiconductor elements diffused in the same silicon chip and the resulting parasitic capacitances.

b) Difficulty in maintaining resistor tolerances better than approximately 20%.

c) Difficulty in fabricating capacitancies of more than a few micro-microfarads.

During the past two years significant progress has been made in developing isolation techniques so that this is no longer a serious drawback. High tolerance or value resistors and capacitors can be deposited on the monolithic silicon chip by thin-film deposition techniques. There is no known method of fabricating inductors, but fortunately this presents no problem for digital circuits.

It is difficult to get accurate information on the yield experienced by manufacturers, but estimates range from approximately 2% to 30% for present high-grade military type circuits depending upon the type and complexity of the circuit.. Yields of 50 to 90% are predicted for the future. Propagation delays in the order of 1 to 3 nanoseconds are available today. Present state-of-the-art permits approximately 100 to 200 components on a single chip in production devices. These figures should increase to over 1000 by 1970. Discretionery wiring techniques may increase these figures further.

Monolithic integrated circuits are well suited to digital applications where component values are not as critical, but they are less satisfactory than hybrid or discrete circuits for most types of linear circuits because of the interactions and the difficulty in controlling tight tolerances. Intensive research and development efforts during the past two years have lead to significant progress in linear monolithic integrated circuits. [62, 63.] Bipolar monolithic integrated circuits are expected to be the major integrated circuit technique used in digital applications, including shipboard data systems, within the next few years. In addition to the use of thin film techniques for fabricating the necessary interconnection patterns on large arrays of bipolar circuits, thin-film resistors and capacitors can also be deposited on the silicon circuitry to fabricate higher value or higher tolerance resistors and capacitors

when necessary. [64.] Several hundred thousands ohms of resistance and several hundred micro-microfarads of capacity can be obtained on an integrated circuit in this way. Resistor tolerances are better than 10% and capacity tolerances of two parts per million can be obtained easily. [65.] "Trimming" the resistor during test operation can provide even higher tolerances. The ability to achieve these characteristics are of particular importance in linear circuits, such as memory sense amplifiers. [35] In addition to logic elements, bipolar integrated circuits are also being used as scratch-pad memories. One commercially available computer uses up to 512 words of 150 ns integrated storage fabricated with integrated circuits containing eight bits of storage per chip. [66.] Another scratch pad memory operating at 27 ns for a complete cycle and a 17 ns non destructive read cycle has been described. [67.]

4.2 Metal-Oxide-Semiconductor (MOS)

In this type of device single diffusion process is required in a silicon chip. [68.] This is a field-effect device in which metal electrodes are deposited on two slightly separated diffused areas (e. g. N type material for a P type chip), an insulator (e. g. silicon monoxide) is deposited on the chip between the two diffused areas, and the third metal electrode is deposited on the insulator.

Although MOS devices have advantages from the fabrication standpoint, they cannot match the 2 to 3 ns speeds quoted for bipolar transistors. Present work with MOS devices indicate potential speeds in the order of 50 ns. Since significantly fewer processing steps are involved, the fabrication of large arrays of elements with reasonable yields is more feasible. In contrast to bipolar transistors, MOS elements are high impedance devices. The following advantages have been cited for MOS devices:

a) There is no problem with "current hogging" in DCTL type circuits.

b) High fan-out can be obtained.

c) Complementary symmetry circuits can be made on the same substrate with only one extra diffusion process.

d) They are simple to fabricate and large arrays of circuits can be fabricated with higher densities and yields.

Complementary symmetry devices have been fabricated by diffusing areas of N type material into the P type substrate, then diffusing P type material into the N type areas.

Complementary symmetry permits one MOS transistor to be used as a load switch for the other. This increases the reliability and radiation resistance since shifts in the characteristics of the devices have a lesser effect if the load line is the characteristic of another MOS rather than a straight line resistor type load. As the characteristics of one MOS change, due to external conditions, the characteristics of the other change also, resulting in a lesser circuit effect from the net change. However, inherent radiation resistant advantages that have been claimed for MOS devices, because they are majority carrier devices, have been largely discredited. [69, 70.]

Most companies have experienced a surface instability in metal oxide semiconductors that is very temperature dependent, but this appears to have been overcome during the past two years. It has been reported that this surface instability, caused by charge motion at the metal-to-oxide interface (charge leakage around the gate), can be overcome by phosphorous treating of the surface. The need for controlling the thickness of the diffusion layer in bipolar circuits is traded for the need to control the thickness of the oxide in MOS circuits. It is not clear that this will be an advantageous trade for MOS devices.

MOS devices can be fabricated with densities approximately four times that achievable with bipolar devices today. However, this density advantage will probably decrease to perhaps 2:1 as isolation techniques for bipolar devices are improved and as densities for both types of

devices are increased to the point that the area required for inter-
connections becomes a major factor. [42.] The speed of MOS devices
can be improved by using "N-channel" and "P-channel" MOS devices
in complementary circuits, but this requires more complicated pro-
cessing steps and reduces the density achievable with MOS devices. [71]
MOS arrays have been used for random access scratch-pad memories,
associative memories, [72, 73] DDA integrators, [74] and shift registers. [75]
A 128 X 64 bit MOS memory has been successfully operated with a 35
nanosecond read cycle time and a 60 nanosecond write cycle time with
standby power of only 0.1 milliwatts per storage cell. [71] The low
power requirements of MOS memories makes them attractive for space-
borne and other low power applications. In the DDA integrator
230 MOS devices are fabricated on a single 72 by 86 mil chip. [74] A 100
bit shift register containing 615 MOS transistors has been fabricated
in a single 100 by 65 mil silicon chip. [75] Because of the higher circuit
complexity that can be achieved per unit of chip area, it is likely that
MOS devices will be used in future systems where speed is not impor-
tant. However, in most computer applications higher circuit speeds
result in higher system performance; hence, MOS circuits will have
difficulty competing with bipolar circuits in most applications. Appli-
cations where the required circuit speed is limited by external factors,
such as interfaces with electro-mechanical equipment or manual opera-
tions, will be more attractive areas for MOS arrays. Small serial
computers may be another attractive application for MOS arrays. [76]

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5. LSI CONSIDERATIONS

Large-scale-integration (LSI) has dominated research efforts and technical discussions in the components and packaging field during the past two years. The term "LSI" is commonly used to designate large arrays of integrated circuits with hundreds or thousands of gates or other circuits interconnected on a single silicon chip. LSI is important not only in decreasing the cost of individual circuits but also in decreasing the cost and increasing the reliability of interconnections between circuits and decreasing packaging and assembling costs. In the material prepared in 1964 for the final ANTACCS Report emphasis was placed on the progress in monolithic silicon integrated circuits., and it was indicated that research and development efforts underway at that time indicated a strong likelihood that integrated circuit technology would ultimately permit fabricating many circuits and their interconnections on a single chip. Progress in LSI has been more rapid in the past two years than anticipated. At this point it seems almost certain that arrays of over 100 circuits will be in use in operational systems by 1970 and that arrays with over 1000 circuits will be in operational use by 1975, and possibly earlier.

While semiconductor and device specialists are wrestling with problems of material and fabrication techniques for LSI, machine organization and computer systems specialists are wrestling with the problem of how to use large arrays effectively in computers and other digital systems. In considering large scale integration one is faced with two major problems:

      1. The possible need for eliminating bad or sub-standard circuits from the arrays to achieve a reasonable yield by avoiding the requirement that 100% of the circuit on a chip be perfect.

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2. The lack of flexibility resulting from large arrays which tends to make each array within a system unique and which tends to require either common use of standard arrays by many customers or increased cost for customizing arrays.

These problems and their probable effects on future systems designs will be discussed in this section. Unfortunately, present machine organization approaches do not lend themselves well to the highly modular design and fabrication techniques necessary to permit efficient utilization of LSI by minimizing the interconnections between arrays.

Integrated circuit arrays containing in the order of 20 circuits per chip are commercially available now and the next generation containing in the order of 100 circuits per chip is now under development.[77] There is no clear indication at this time as to what the ultimate limit will be in the number of circuits per chip, but as many as 1000 logic circuits per chip by 1970 has been predicted.[78] It appears reasonable to expect that arrays of at least 2000 to 5000 circuits per chip will be feasible ultimately. The question of array size for LSI depends upon many factors other than processing techniques and their feasibility. Other major factors that will affect the useful size of LSI arrays include yield, cost trade-offs, quantity of a particular array determined by requirements for customizing arrays, ability to organize the computer functionally to use large arrays without excessive interconnection requirements, and repairability and maintainability considerations.

Both bipolar and MOS techniques are adaptable to LSI with MOS presently having the edge in array size. MOS devices presently have a density advantage also, but as higher and higher element densities are achieved in both techniques, the space required for

interconnections between circuits in the array will ultimately become the limiting factor on density. Also, as densities increase, the lead delays in connections between circuits will become smaller, thus placing a greater premium on the inherent speed of bipolar devices. However, in general the advantages and problems of LSI are similar for bipolar and MOS techniques. Hence, in the remainder of this appendix, LSI considerations will be discussed independently of the device technique used on the assumption that ultimately bipolar devices will be used where they are most advantageous and MOS devices will be used where they offer advantages.

The Air Force is presently sponsoring three competitive development contracts that will provide some answers to the questions of how to organize machines for effective use of large arrays, how to achieve yield and flexibility in these arrays, and whether MOS devices, bipolar devices, or a combination of these is the better approach. The problems and goals of this study stated in the initial request for proposal, are quoted below because of their interest to this consideration of LSI:

> 1. <u>STATEMENT OF THE PROBLEM</u>: The successful development, and subsequent production of silicon integrated circuitry, has proven this technology capable of providing an order of magnitude improvement in reliability of systems utilizing this approach. Concurrent with this improvement in reliability has been a continuing reduction in circuit function cost. This reduction has progressed to the degree that package cost for these circuit functions represents approximately 50% of the final cost. It has been further shown that the intrinsic reliability of the silicon integrated circuit (SIC) is at least one more order of magnitude higher than that which is achievable with the circuits after individual packaging. This indicates that predominant failures are associated with bonding and lead failures within the circuit and multilayer wiring board or interconnection failures at the system level. These failures can be further eliminated by reduction of the circuit to circuit transfers required external to the silicon wafer and concurrently a reduction in the number of connections required at the subsystem level.

This in turn will greatly reduce the number of individual
packages with their associated input-output terminations.
Thus it is readily apparent that if these higher order cir-
cuit functions can be achieved, today's level of reliability,
cost and size reduction can be further improved. It is
the objective of this program to develop the technology
for such an approach.

2. OBJECTIVE: It is the objective of this program to
accomplish as much as a ten to one improvement in relia-
bility in electronic subsystem or systems over that pres-
ently available with today's integrated circuit capability.
It is a further objective to achieve this improved reliability
while simultaneously achieving enhanced subsystem per-
formance and an overall cost reduction. These improve-
ments will be accomplished through the sophisticated use
of a large scale monolithic integrated circuit array con-
taining up to 1,000 circuits utilizing either metal-oxide -
semiconductor (MOS) or bipolar active devices with
associated passive elements capable of being intercon-
nected to perform logic for data processing, memory,
and/or analog functions.[79]

One of these contracts is using bipolar techniques, one MOS techniques,

and one a combination of bipolar and MOS techniques.

References 42, 46, 80 and 81 are of particular interest in considering

the system implications of LSI. An article by R. Rice entitled "Impact

of Arrays on Digital Systems" to be presented at the 1966 Solid-State

Circuit Conference is also significant.

5.1 Cost Consideration

LSI will tend to reduce electronics by permitting the fabrication of a

large number of circuits in a single set of processing operations, by per-

mitting the fabrication of the interconnections between these circuits in a

batch-fabrication operation (vacuum deposition) and by amortizing the

packaging costs over a larger number of circuits. However, a number of

different considerations affect the extent to which these apparent cost

reductions can be realized in practice. One of the most important of ths

is yield. The actual fabrication or processing costs are relatively inseni-

tive to array size and complexity except for the yield problem. However,

as array size and complexity increases, it becomes increasingly difficult to maintain a given yield since all of the components and circuits in the area must be good. This is particularly true when the increase in complexity calls for an increase in the physical size of the array. Hence, at any given point in the development of device technology, there will exist some array size giving minimum cost per component where low yield will make larger arrays more expensive per component and packaging and fabrication costs will make smaller arrays more expensive per component.

The cost of large arrays will also be affected by tolerance requirements, achieveable densities, and testing requirements. Testing is a particularly important consideration for large arrays because of the astronomical way in which the number of possible combinations increases with the number of logical elements if exhaustive tests are to be used. For example, exhaustively testing every combination of a 10 by 10 array of binary elements would require 2^{100} different tests - an obviously unreasonable number. A requirement for testing individual circuits or groups of circuits within the array also implies a requirement for testing pads which use relatively large amounts of area. This in turn increases lead lengths and decreases density, thus tending to limit the size and complexity of the array for a given chip size. Ultimately, it will be necessary to develop functional tests for large arrays which require access to only a limited number of test points within the array. However, considerably better control of processing steps and better quality control may be required before this is feasible.

While the fabrication cost advantages of large arrays provide strong incentive for putting more and more logic on a single chip, practical considerations of standardization, customization, and system

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systemorganization, tend to limit the desirable array size because
of the relatively high start-up cost for each different type of array.
The cost of producing large arrays can be divided into three major
categories;

1. - Fabrication costs - e. g. labor, materials, etc.
2. - Fixed costs amortized over all units - e. g. facilities,
     process and technology development, etc.
3.- Custom costs att ributable to each new type of array -
     e. g. array design, test design, mask-making, etc.

In the recent past, start-up costs of custom designed integrated
circuits have amounted to approximately 30% of the total cost.
Because of the higher production volume of standardized circuits,
start-up costs have accounted for about 10% of the total cost of
standardized circuits. In either case, an increase in the number
of different types of arrays combined with the decrease in the
total number of arrays as size increases will increase the effect
of start-up costs significantly. Hence, it is clearly necessary
to minimize the number of different types of arrays by using
some standardized arrays and to develop design and fabrication
techniques that will reduce the cost of customizing arrays.
Integrated circuits have already minimized the previous tendency
for each engineer to design his own flip-flop in favor of a relatively
small number of semi-standard integrated circuit flip-flops. The
same trend toward standardization will be necessary for larger
units (e. g. a complete arithmetic unit) in the future. Memories
are a particularly attractive application for LSI because of the ease
of standardizing large storage areas.

One approach being taken to alleviate the problem of start-up costs
for customized areas is to develop large array chips, consisting of
many standard circuits, which are identical up to the final layer of

metalization. In this approach only one special mask is required to customize the array to a particular function. However, penalties are paid in terms of lesser densities and not being able to optimize the design of individual circuits for specific requirements. Some- what greater flexibility can be achieved, if necessary, by customiz- ing the two final layers of metalization.

The highest cost for customizing an array occurs when the basic circuit is changes. Hence, using a standardized circuit and customizing only the interconnections,will significantly reduce start-up costs. Dr. Noyce summarized this problem well by stating.

> "Only standardization, plus the development of automatic
> design capabilities, will make integrated arrays available
> in the future at a substantial cost reduction compared
> with today's integrated circuits. "[80]

Past experience in the computer field indicates that it will be very difficult to get different manufacturers to standardize large functional arrays, such as a complete arithmetic unit, even within a single company, much less between companies. Only long-range economic considerations can force this in the commercial computer industry. However, as a major customer, the Government is in a position to do something about this problem for military systems by sponsoring the development of a family of large arrays from which major portions of many different kinds of computers and digital systems can be fabricated and insisting on the use of these arrays in future procurements. Standardization efforts by government agencies should no longer be pointed toward the circuit or sub-function level where it has always been difficult to specify circuit and packaging techniques applicable to all functions and types of equipment without overdesigning the circuit.

Instead, standardization efforts should be directed toward development of large functional arrays that can serve as major building blocks in many different types and sizes of computers and digital systems. The disadvantages of using a large array which is in itself not optimum for a particular system will be out-weighed by the low cost of the standardized array and the minimization of external connections permitted by the larger array.

5.2 Yield

The yield achieved by different manufacturers is one of the most closely guarded secrets in the integrated circuit field, but, in general, yields are believed to run between 25% and 50% for production circuits. However, because of the larger size, LSI yields will be significantly lower for the foreseeable future. Hence, yield is a major consideration in the design and utilization of LSI, arrays. Yield is also an important consideration with respect to reliability since very low yields imply poor control of the fabrication process and inadequate quality control. These, in turn are very likely to cause poorer reliability during the life of the array.

Because of the large number of circuits in an LSI array, and the consequent reduction in the cost per circuit, lower yields can be tolerated with LSI than with smaller integrated circuits. However, the yield must be sufficiently high to permit adequate fabrication cost reductions to compensate for the lack of flexibility and higher start-up costs. One approach to achieving higher yield is to concentrate efforts on process improvements and require all circuits within an array to be good. Some semiconductor companies are taking this approach in the beliefs that they can improve process technology sufficiently to make LSI feasible.

Another approach is the use of "discretionary wiring." In this approach the individual circuits are tested and a computer is used to design an interconnection mask to connect the good circuits into the proper logical configuration while eliminating the bad circuits. This requires space for test pads for the individual circuits which may use more area on the chip than the circuits themselves. It also requires computer time and the preparation of a specilized mask for at least the final layer of metalization for each array. At any given point in time, the state-of-the-art of processing technology will permit a larger array with discretionary wiring techniques than in any approach that requires that all circuits on the chip be good, Hence, discretionary wiring is advantageous in cases where it is necessary to push the available state-of-the-art with respect to array size. Which approach will win out is a controversial question within the semi-conductor industry. However, it seems likely that in the long run processing technology will permit reasonable yields in fabricating large arrays in which all circuits are good. Because of the lesser costs involved for each array, the yield in this approach would not need to be as high as that for discretionary wiring. It would be comforting to believe that processing steps were sufficiently under control to permit an adequate yield while requiring that all circuits in an array be operable. Although discretionary wiring may be questionable from the standpoint of yield improvement, this technique may prove very valuable in permitting the customizing of arrays.

Discretionary wiring techniques are being pursued actively by one or more companies in the semiconductor field, while others are emphasizing process improvements to achieve sufficiently high yields to permit the use of fixed interconnect pattersn. The Air Force is sponsoring work on discretionary wiring under one contract in which unit cells, consisting of NAND gates or flip-flops are tested and

interconnected by discretionary wiring techniques.[82] A first level of metalization provides test pads which permit testing of the circuits and introduction of the test results into a computer which generates an interconnection pattern. A cathode-ray-tube is used to project this pattern to form a photo-mask, which, in turn, is used to fabricate the interconnection pattern on the chip.

It is important to note that the advantages of discretionary wiring over fixed interconnection arrays from a yield standpoint will tend to decrease with time as the yield of processing steps improves. On the other hand, the importance of discretionary wiring from the standpoint of customizing arrays is likely to increase as array size increases.

5.3 Flexibility and Customizing

One of the major problems that will tend to inhibit the widespread use of LSI is the difficulty of achieving flexibility in the logical configuration of large arrays. Techniques for economically changing the logical configuration of a large array during fabrication and machine organization and a system design and approaches to minimize the different types of arrays required will be needed. Requirements for flexibility are imposed by four major factors:

1. With very large arrays it will be difficult to achieve multiple use of a single array design within a given computer. If a computer is fabricated with 20 large arrays, it is very likely that these will be unique.

2. Different sizes and types of computers and other digital equipments require different logical functions and configurations.

3. Different manufacturers want different array designs even for similar classes of equipment.

4. Engineering changes, particularly in the early stages of production, will require the ability to either change an existing array with jumper wires or, preferably, to easily and cheaply fabricate a new array.

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Hence, even if sufficiently high yields are obtained for large arrays to permit fixed interconnect patterns, economical means for changing the interconnect pattern still will be required because of the four considerations listed above. Significant progress is being made in design automation techniques that will facilitate the computer generation of wiring patterns, but the ability to fabricate interconnection masks cheaply will also be required. In the long run, this may be the most important contribution of the work presently underway on discretionary wiring. Discretionary wiring to improve the yield problem essentially requires the generation of a new mask for each array depending upon the specific location of bad circuits in the array. On the other hand, discretionary wiring for flexibility and customizing of arrays requires the generation of a new mask only for each different array configuration or logical function. Thus, discretionary wiring techniques that would be almost prohibitively expensive for yield improvement would have only minor cost effects when used for customizing arrays. To keep the start-up and change-over costs low in customizing arrays, it is essential that the differences occur only in the interconnections between gates wherever possible and only infrequently in the wiring of the elements into gates or flip-flops. Changes in the basic design of the elements (e.g. size, different processes, etc.) must be avoided. The cost of changing the interconnection pattern between gates is in the order of $500, while the cost of changing the way in which the elements are wired into gates or flip-flops costs between $1500 and $5000. Changing the basic design of the element costs in the order of $50,000 to $100,000. Hence, if the changes required in customizing circuits or making engineering design changes can be limited to the interconnection pattern only, adequate flexibility can be achieved economically by design automation and automatic mask making techniques.

In order to minimize the cost of changes in array configuration and to reduce the "turn-around" time. Careful attention must be given to the interface semiconductor vendor and the user or system designer.

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Approaches to this interface have been described in the literature. [83,84] One of the major considerations in this interface is the design and specification of tests based on an intimate knowledge of failure modes and the specific interconnection patterns. The user must resist the temptation to over specify exhaustive test.

5.4 Interconnections

The ability to achieve the cost and reliability improvements offered by LSI is limited to a very large extent by the interconnection problem. Intraconnections between circuits on a single chip can be made cheaply and reliably by batch-fabrication processes--e. g. , photo-etching and vacuum deposition. Interconnections between chips require large chip areas for bringing out connection pads and manual or semi-manual operations for connecting the pads to pins and for later connecting the pins to a wiring card. Even with automated wiring techniques and the use of interconnect patterns etched or deposited on glass or ceramic substrates, interconnections external to the chip will constitute major cost and reliability problems. Hence, if LSI is to be used effectively, machine organization techniques are required that permit the machine to be partioned or modularized in a way that minimizes the number of interconnections between large modules.

In general, array sizes within the present state-of-the-art (i. e. , 50 to 200 gates per chip) are in the most awkward size range. Small chips with only a few gates provide a very poor ratio of circuits to pin connections, but the total number of pins required on a module can be fabricated relatively easily. For much larger arrays containing hundreds or thousands of gates, a large percentage of the connections can be made internal to the chip. This permits a much better ratio but the total number of leads required will be prohibitive for conventional maching organizations.

An analysis of a number of recent commercial computers with 10,000 to 30,000 gates each indicated that the gate-to-pin ratio would average 0.7 to 1 if the system were partioned into arrays of 20 gates each and that this ratio would increase to 1.4 to 1 for 1,400 gate arrays. [85.] Although this represents an improvement by a factor of two for the larger array, the total number of pin interconnections for the 1,400 gate array would be approximately 1,000. This problem is more severe in the control portion of the machine due to the irregular nature of the control function and previous emphasis on reducing the total number of gates in the machine. The arithmetic functions lead to much more regular configurations with fewer connections required.

One approach to reorganizing a computer to reduce pin connections rather than gates by distributing parts of the control function among different modules led to 80% fewer pin connections improving the gate-to-pin ratio to 7.2 to 1 for the control functions. [85] Much more research work along these lines is needed to minimize the control signals between modules. With very large arrays it should be possible to require pin connections only for input and output data lines and a very limited number of major control signals. For example, a complete 25 bit arithmetic unit would require only 85 pins. This can be accomplished by using cheap LSI gates lavishly and redundantly in each module to repeat decoding functions and the generation of control signals. A complete computer on a single silicon chip is an extreme example of this goal. For the near future, 200 gates in a 50 pin package seems to be reasonable and achievable goal. This apparent ratio of 4 to 1 is somewhat high since some of the gates will be unused in a practical application.

The physical problem of connecting large numbers of leads to the
device in an LSI array and the system problems of adverse cost and
reliability effects of pin interconnections lead to a strong need for
minimizing the number of external pin connections required Hence,
minimization of interconnections must replace minimization of
gates as a major design criteria for LSI systems.

5 5 Reliability and Maintainability

It seems apparent that LSI will significantly improve the reliability of
future systems by reducing the total number of component parts and
by exchanging external interconnections for more reliable
intraconnections fabricated directly on the
silicon chip Even if the statement sometimes made by integrated
circuit experts in the semiconductor industry that the reliability of
a complete circuit (and perhaps an array) will approach that of a single
discrete transistor is somewhat exaggerated, very significant relia-
bility improvements will be achieved.

LSI will also serve to lower the cost of redundancy used to improve
reliability, but it is questionable whether this will be necessary for
other than the most demanding applications such as deep space probes.
For any given level of component or device reliability, redundancy
techniques can improve equipment and system reliability, but the
advantages of this tend to decrease as basic component reliability
increases. It is unlikely that redundancy techniques would be required
for most applications if the complete computer were fabricated with
20 LSI arrays each having a failure rate in the order of 0. 001% per
thousand hours '

Several different redundancy techniques have been described in the
literature [86, 87, 88, 89] These include redundancy at the basic
component level, logic circuit level, function level, equipment level,
sub-system level, and system level LSI will also make feasible

self-repairable systems in which spare or standby units can be connected automatically to replace failed units.[90] The most attractive place to use redundancy with LSI is within the array where redundant components, circuits, or functions can be wired with their "voting" circuits right on the same chip, thus not increasing the number of external interconnections. However this is not as satisfactory a solution as it appears at first glance since the failures within an array may not be independent -- the cause of one failure is more likely to cause others. On the other hand redundancy between arrays increases the number of external interconnections and may reduce the system reliability by more than that gained through the use of the redundancy. For Naval tactical systems the use of large arrays in a non-redundant manner will provide adequate reliability -- probably between one and two orders of magnitude improvement over present systems. Further reliability improvements should be made at the equipment and systems levels by systems design approaches (e. g., multi-computer or parallel processor systems) that modularize the systems capability providing for rapid replacement of failed units and continuous operation of critical functions by "graceful degradation".

Integrated circuit reliability will increase to the point that most failures in the computer will result from interconnections and packaging problems Reliability workers concerned with the APOLLO computer have reported finding no inherent failure modes, but a large number of failure modes have been found that result from fabrication flaws, human errors, and poor quality control. All failure modes that have been discovered are said to be "the result of poor process control or the vendor's lack of complete technical knowledge of his process. Most problems are quality control problems. There is no substitute for good, tight inspection on the line." [91] The fact that failures are largely the result of poor quality and process control was dramatically illustrated

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by a table comparing the test results and failure rates for three different vendors manufacturing the same integrated circuit type for the APOLLO program. This table, presented by Partridge, at the ONR sponsored conference on Microelectronics and Large Systems, is reproduced below:[92]

Vendor	Pre-Qualifications % Failures	Screen & Burn-in % Failures		Failure Rates At Use Conditions 90% Confidence
		Total	2nd & 3rd Electrical	
A	5	1.8	0.3	$0.005\%/10^3$ Hrs. (0 failures)
B	26	3.8	1.7	$0.3\%/10^3$ Hrs. (2 failures)
C	58	5.0	2.5	$1.8\%/10^3$ Hrs. (26 failures)

It is interesting to note that the relative position of the three vendors were maintained at all four steps in the evaluation.

Since most monolithic semiconductor integrated circuits are fabricated in the same manner and with the same processes as the silicon planar transistor, most workers in the field expect the failure rate of an integrated circuit to approximate that of a single discrete transistor of comparable die size.[93,94] In fact, Platzek and Goodman state:

> "Because these circuits are fabricated in exactly the same manner as the silicon, planar, passivated transistor, it is reasonable to exploit the test data acquired from the Minuteman high reliability component program. ...Recent published data supports the position that semiconductor integrated circuits will have failure rates closely approximating those of individual discrete transistors."[94]

Bridges (of the Department of Defense) states that "a semiconductor integral circuit containing the equivalent of some 20 parts displays the same failure rate as a single conventional transistor", and he

predicts failure rates of approximately 0.0001% per 1,000 hours.[95] A number of estimates place the ultimate reliability of monolithic integrated circuits in the order of 0.0001% failures per 1,000 hours.[94,95,96] Acutal experience to date appears to be running between 0.01 and 0.005% failure per 1,000 hours depending upon the manufacturer and the type of circuit.

In view of both long range predictions and recent actual experience, failure rates in the order of 0.001% per thousand hours or better are reasonable expectation for the early part of the 1970-1980 era. Such failure rates should provide one to two orders of magnitude higher systems reliability for the central processor and other digital electronics portions of Naval tactical systems in that time frame. This, of course, assumes that the equipment is organized in a way to permit the effective use of LSI arrays. It is also important to note that electromechanical peripheral equipment and, to a lesser extent, displays will limit the improvement in overall systems reliability.

The combination of greatly reduced failure rates and large functional modules using LSI techniques will have a major impact on the maintainability of Naval tactical systems during the next decade. Maintainability improvements are discussed in greater detail in Section 4 of the body of this report. A maintainability concept is proposed that is based on very large functional throw-away units and no shipboard or field repair of modules. Maintenance for the digital electronics portion of the system would consist of fault isolation to one of a limited number of large modules by a diagnostic program and repair by merely replacing the large module. Since making an LSI array repairable would require reducing its circuit density and complexity, the failed unit will be thrown away. The low failure rate will make this economically feasible. Logistic, personnel, and training requirements will be reduced.

6. PROBLEM AREAS

Many problems remain to be solved in processing techniques and device technology before LSI arrays with the size (complexity), cost, and reliability discussed in this report become feasible for volume production and operational use in the field. However, progress to date gives every reason for confidence that the semiconductor industry will successfully solve these problems. There is less reason for confidence that the computer industry will successfully solve the machine organization, systems design, and applications problems raised by the imminent availability of LSI.

Most of these problems have been discussed throughout this report, but a few of the more important ones are summarized here for emphasis. These include:

Development of machine organization techniques that will permit partitioning the system to:

Minimize interconnections between large arrays,

Permit repetitive use of similar arrays within a system

Incentives for industry wide use of similar arrays for similar functions in different equipments and different types of equipments.

Development of appropriate interfaces between semiconductor manufacturers and computer manufacturers to permit each to best fill the functions in their areas of specialization while reducing turn-around time and improving final system cost and performance.

Development of discretionary wiring or other techniques for economically customizing large arrays and handling engineering changes.

Changes in design attitudes and objectives to permit logic to be used "inefficiently" to minimize interconnections rather than the gate or flip-flop count.

Use of LSI arrays and internal batch-fabricated storage to reduce software complexity and cost and to reduce the need for electromechanical peripheral equipments.

Development of techniques for adequately testing large arrays while keeping testing times and costs within reason and without decreasing the array complexity to provide large areas for internal test pads.

Development and acceptance of maintainability concepts that use large throw-away modules in order to avoid introducing additional partitioning and artifical segmentation of modules to facilitate repairability of a module.

In the meantime it is hoped that the semiconductor industry will fulfill its promise of solving the problems of yield, quality control, and automation of mask making.

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Appendix B
MEMORY TECHNOLOGY

1 GENERAL

In any future naval tactical system, memories and storage devices will be required for a number of different functional uses each of which places different requirements on the memory technology in terms of the necessary characteristics or combination of characteristics. Some memory technologies are applicable to only one functional use while others are applicable to several. These functional uses of memory and storage devices include discrete bit storage, registers, high speed control or scratch pad memories, main internal memories, on-line auxiliary storage, and off-line auxiliary storage. In addition to these major functional categories, there are several other types of "special purpose" memories such as read-only memories, read-mostly memories, and associative memories. The majority of the effort during this study has been devoted to the major functional categories of memories listed. Only limited consideration has been given to special purpose memories since their utilization in future naval tactical systems is uncertain and depends upon the design approach taken and specific decisions of system planners.

This appendix discusses technical developments affecting each of the functional categories of memories and storage devices and evaluates the future characteristics anticipated for each of the major memory technologies presently under development that appear to be likely contenders for use in naval tactical systems in the 1970-80 era. Most of the memory technologies discussed here were previously covered in the material prepared in 1964 for the ANTACCS Final Report, but this appendix reflects the results of the continuing research and development efforts in these technologies during the past two years.

Several that have not proven out have been dropped from consideration. No new ones have been proven sufficiently promising to justify adding them.

Batch-fabrication techniques provide the key to achieving lower costs, higher reliability, smaller size and weight, faster speed, and lower power requirements. Hence, whether a particular memory technology involves batch fabrication is a major criteria in its evaluation for use in future systems. For future memories, batch-fabrication techniques will be important both in the fabrication of the memory or storage array itself, and in the fabrication of the electronics associated with the memory--the address circuits, selection circuits, drivers, sense amplifiers, etc. The integrated circuits techniques discussed in Appendix A will undoubtedly provide the batch-fabricated electronics necessary for use with the memory technologies discussed in this appendix as well as providing the storage elements themselves in MOS and bipolar integrated circuit array memories.

Memory technology is advancing rapidly as a result of both continuing improvements in magnetic core technology and the development of new memory technologies utilizing batch-fabrication techniques.

During the time between 1970 and 1980, continual improvements will be made in the characteristics of most of the memory types covered in this study. Other types of memories not feasible for a 1970 system will probably be developed to a point that they can be included in an operational system by 1975 or 1980. There will undoubtedly be some radically new memory techniques developed during the 1970-80 period, but a large part of the improvement in memory characteristics and capabilities during that time period will result from continued

improvements of memories now in use or under development. This is particularly true with respect to improved batch-fabrication techniques. It is possible that some exotic new memory techniques, such as a high-speed random access read/write memory based on the use of lasers, will be developed during that time period, but it is certain that new methods of fabricating magnetic and integrated circuit memories will be developed that will have significant and dramatic effects on the cost, speed and capacity.

In the past, anticipated advantages of new memory technologies, such as magnetic thin-films or cryogenics, were based on their enhanced characteristics over those anticipated for core memories. Unfortunately for other technologies, core memory technology has advanced so rapidly that by the time the proposed characteristics of the other storage devices were realized, equal or better characteristics were available from magnetic core memories. In view of this past history, it is dangerous to predict that core memories will be replaced by other technologies by a given date. On the other hand, it is difficult to believe that these advances in core memory technology can be continued indefinitely. Additional advances in magnetic materials and semiconductors can be anticipated, but it is unlikely that the size of discrete cores can be reduced significantly below 12 mils OD and 7 mils ID and still permit the threading of addressing and sensing wires. As a result, magnetic core memories will eventually give way to newer technologies.

For any new technology to replace an established technology with 15 years of cumulative development and operational experience, the new technology must inherently offer significant advantages over the established magnetic core technology. Significant advantages over

the established magnetic core technology are most likely to result
from the batch-fabrication aspects of other memory technologies.
Techniques for fabricating large memory arrays as units, rather than
by assembly of large numbers of discrete elements, are well along
at this time and are receiving considerable attention from the industry.
The memory function is particularly adaptable to batch-fabrication
techniques since it consists of large numbers of similar elements and
hence is highly repetitive. This is true on one extreme for small
high-speed one-word registers that might be fabricated as a single
integrated circuit array, and on the other extreme for large capacity
on-line auxiliary memories. It is certain that techniques of this type
will be feasible, economic, highly developed, and in widespread use
by 1970. Batch-fabrication of logical and memory circuitry and of
arrays of storage elements will be the key factor making possible more
capable and sophisticated computers with greater reliability, lower cost,
and smaller size, weight, and power requirements.

However, even with batch-fabrication large capacity solid-state on-
line auxiliary memories probably will not be competitive with electro-
mechanical auxiliary storage (e. g. , magnetic disc files and magnetic
card memories) on a cost-per-bit basis by that time. It may be
necessary either to use some electromechanical device for large
mass memories, or to recognize and accept a cost penalty for using
a solid-state device in order to obtain much faster access times or
more desirable characteristics for military environments. This is
particularly true for mass memories with capacities of 109 bits and
above. Although these very large capacities can be achieved by using
multiple banks of smaller memories, this usually is not economically
feasible. As a result, moving magnetic-media type electromechanical
memories will likely be used for capacities of 109 bits and above for the
foreseeable future.

2 FUNCTIONAL TYPES OF STORAGE

Almost all computer systems use a combination of several different
types of storage devices in a storage hierarchy to achieve necessary
capacity and speed at a reasonable cost. A compromise solution to
the desires for a very large capacity, very high speed, and very low
cost memory is achieved in such a storage hierarchy by using each
different type of storage in a way that minimizes its disadvantages and
maximizes its advantages. Expensive high speed storage can be used
in small quantities and cheap low speed storage in larger quantities.
The functional types of storage that are expected to be used in computers
for future naval tactical systems include the following:

Discrete bit storage - for temporary storage of indicators,
control signals, and results of previous operations or
logical functions;

Registers - for temporary storage of data and instructions,
for implementing control functions or arithmetic and
logical operations, and for addressing larger memories;

High-speed control or scratch-pad memories - for multiple
arithmetic or control registers for buffering and matching
data rates between devices and for temporary storage of
intermediate results, frequently-used data, constants,
and short subroutines which are being iterated;

Main internal memories - for storing data and instructions
of the program currently being executed for storing
alternate programs that may be needed rapidly in the event of
a real-time interrupt, and for buffering input/output data;

Solid-state auxiliary on-line storage - for storing tables,
data, and alternate programs that may need to be recalled
into main memory rapidly;

Electromechanical auxiliary on-line storage - for storing
large data files and programs that may be recalled by
the computer but where speed is less important and capacity
and cost are more important than for solid-state auxiliary
storage;

Off-line auxiliary storage - for storing very large data files
and large program libraries which are used sufficiently

infrequently to permit a manual operation to make the
storage available to the system.

There are, of course, many other uses for most of the levels of
storage listed above, (e. g. , for control functions and buffering in
displays, communication equipment, and input/output equipment), but
the ones stated are typical of their major functional uses. Different
combinations of speed, capacity, cost, and other characteristics are
required for each of these functional categories of storage. A
specific memory technology may overlap two or more categories, but
the relative importance of the different characteristics and, to some
extent, the design approaches and criteria vary from one category
to another.

The seven functional memory categories listed above will be combined
into four categories for purpose of discussion in the remainder of
this appendix. Discrete bit storage and registers are covered under
integrated circuits in Appendix A. Electromechanical on-line
auxiliary storage devices such as magnetic drums, discs, cards, and
tape loops are grouped with off-line electromechanical auxiliary
storage devices that use magnetic surface recording techniques.
Other electromechanical devices, such as punched cards, punched
paper tape, and incremental magnetic tape, that may be used either
as off-line auxiliary storage or as input/output equipment are
discussed with other input/output equipments in Appendix D. Hence,
the remainder of the discussion in this appendix will consider four
categories--high-speed control and scratch-pad memories, main
internal memories, solid-state on-line auxiliary storage, and electro-
mechanical auxiliary storage.

The high-speed control memory and the high-speed internal memory
are normally considered an integral part of the computer or central
processor, while the on-line auxiliary storage, and the equipment
for reading and writing the off-line auxiliary storage, may be con-
sidered external peripheral devices. Techniques used in mechanizing
registers and high-speed memory in the central processor are also
used for control and buffering functions in peripheral devices. This
is illustrated by the use of magnetic core memories as a small
capacity high-speed control memory, as a large capacity high-speed
main internal memory, as a very large capacity on-line auxiliary
storage, or as a small capacity slow-speed buffer in a display unit
or a communication terminal equipment. Although a magnetic core
memory may be used in each of the above applications, the combination
of characteristics designed into the core memory are quite different
for each of these applications.

The auxiliary storage categories represent very large capacity bulk
storage that is usually addressed by the computer in large blocks
rather than by individual words. The average access time is usually
one or more orders of magnitude slower than that of the high-speed
internal memory. On-line auxiliary storage is directly available to
the computer under computer control without manual intervention.
Off-line auxiliary storage normally requires a manual operation to
place the storage media on the read/write devices (e. g. a magnetic
tape unit) that is controlled by the computer. In this sense,
magnetic tape can be considered on-line auxiliary storage if a parti-
cular reel of tape is written, left on the tape unit, and later read
back by the computer. However, if a tape reel is written, taken off
the tape unit, stored on the shelf, and later put back on a tape unit
to be read into the computer again, it is considered off-line auxiliary
storage.

Most off-line storage equipments, such as magnetic tape units, punched paper tape units, and punched card units, are commonly classed as input/output equipment (see Appendix D) since they act as input/output devices to the central processor. Unfortunately, this tends to obscure the fact that these devices are actually serving an off-line auxiliary storage function in the over-all system rather than an input-output function. They should not be confused with "true input" and "true output" devices such as keyboards, printers, optical character readers, voice input devices, voice output devices, analog-to-digital converters, and digital-to-analog converters. (see Appendix D).

Some types of mass memories, such as magnetic card memories and magnetic disc files with removable disc stacks, are on-line auxiliary storage devices with respect to the cards or discs actually on the device at a given time. However, they act as read/write and access mechanisms for off-line storage with respect to cartridges of magnetic cards or stacks of discs on a shelf which have been written by a device previously and will be read by a device subsequently. These devices are discussed with other devices in this appendix, but those that can act as read/write mechanisms for off-line storage are identified.

The present state-of-the-art at the end of 1966 for each of the levels or functional types of storage discussed here is summarized in Table B-1. Typical characteristics are shown for the technology that is presently dominant in each category. These technologies, and others in each category that are expected to be serious contenders for use in future naval tactical systems, are discussed later in greater detail. Advanced technologies for all these types of functional storage, except off-line auxiliary storage, will be considered.

Category	Primary Technologies	Type of Access	Cycle or Access Time	Read/Write Rate	Capacity in Bits	Cost Per Bit
Discrete Bit Storage and Registers	Integrated Circuit Flip-Flop	Random	50 nanosec to 500 nanosec	2 mc to 20 mc	1 to 1,000	$1 to $10
High-Speed Control and Scratch Pad Memories	Magnetic Thin-Film	Random	100 nanosec to 500 nanosec	2 mc to 10 mc	2,500 to 200,000	$0.50 to $2.00
Main High-Speed Internal Memories	Magnetic Core	Random	0.7 microsec to 4 microsec	250 kc to 1.4 mc	10,000 to 2,000,000	5¢ to 25¢
On-Line Auxiliary Storage (Solid State)	Magnetic Core	Random	3 microsec to 12 microsec	83 kc to 333 kc	1×10^6 to 100×10^6	1.5¢ to 3.5¢
On-Line Auxiliary Storage (Electro-Mechanical)	Magnetic Disc File	Semi-Random	15 millisec to 150 millisec	100 kc to 1 mc	20×10^6 to $2,000 \times 10^6$	0.01¢ to 0.2¢
Off-Line Auxiliary Storage	Magnetic Tape	Serial	--	20 kc to 200 kc	--	--

PRESENT STATE-OF-THE-ART
FOR STORAGE DEVICES TYPICAL OF MAJOR CATEGORIES

TABLE B-1

Although some special types of storage, such as read-only memories, [1] read-mostly memories, associative memories,[2] and block-oriented random-access memories (BORAM)[3] may play an important part in future computer systems, they are not covered in detail since their use is not certain but depends upon future system design concepts and future decisions of navy systems planners.

The most likely contenders for different categories of future memories are:

For discrete bit storage and registers:

> Monolithic integrated circuit arrays
> MOS arrays
> Planar magnetic thin-films
> Plated wires

For main internal memories:

> Planar magnetic thin-films
> Plated wires
> Magnetic cores

For solid-state on-line auxiliary storage:

> Plated wire
> Etched-permalloy toroid
> Continuous-sheet cryogenic

For electromechanical on-line auxiliary storage:

> Magnetic disc diles
> Magnetic card files

For off-line auxiliary storage:

> Removable-media disc files
> Magnetic card file cartridges
> Magnetic tape

Optical storage is another possibility for very large capacity on-line and off-line auxiliary storage if reversible recording media are developed to permit alterable (read/write) storage.

3 MEMORY TECHNOLOGIES AND TYPES OF MEDIA

Conceptually, any element or phenomena that exhibits two or more stable states or a delay property can be utilized for storage. However, only a few of these possibilities have proven satisfactory or competitive in the past or offer promise for the future. Means for achieving two stable states include physical, optical, magnetic, electronic, and cryogenic techniques. Examples of these are punched cards, photographic recordings, magnetic cores, flip-flops, and continuous-sheet superconductor storage, respectively. Delays may be achieved by acoustic, mechanical, electronic, or magnetostrictive techniques with the delay media sensed to provide an output which is amplified to regenerate the input signal to maintain recirculation. In general, storage devices based on the use of media with two stable states provide a random access, while those based on the use of a delay media provide a serial access. Magnetic surface storage such as drums, discs, and tapes do not fit neatly into this categorization since the magnetic surface provides two stable states for storing information but mechanical motion of the media is used to provide access and, in the rotating devices, a delay function.

Many different techniques have been used or proposed for internal and on-line auxiliary storage, but only those that are of major importance at present or that are expected to be serious contenders for use in future naval tactical systems will be considered. The more important memory technologies that meet these criteria will be discussed and compared.

3. 1 Integrated Circuit Memories

The most obvious storage application of integrated circuit techniques is in discrete bit storage and registers where each bit position of the

register is mechanized with a single integrated circuit flip-flop.
Registers mechanized with individual integrated circuits are available
operating at cycle times in the order of 50 nanoseconds for repetitive
setting, sensing, and resetting. New developments in integrated
circuits are leading to propagation delays in the order of 2 nanoseconds
per gate, but the complete cycle time for a flip-flop is several
times the propagation delay of an individual gate. Within two or
three years, integrated flip-flops may be available requiring less than
10 nanoseconds for setting and settling. A small scratch pad memory
mechanized with elements of this type is somewhat slower over-all
since some time is required for addressing and selection.

Integrated circuit flip-flops have become the primary method of
mechanizing individual registers in new machines. Advances in the
state-of-the-art will permit the fabrication of entire registers on
a single silicon monolithic integrated circuit chip in the near future.
Transistorized flip-flops have given way to individual flip-flop inte-
grated circuits which will be replaced by multi-stage integrated
circuits within one or two years.

Prototype memories have been developed in which special inte-
grated circuit storage elements are utilized in a matrix con-
figuration. [4] One such element uses a PNP and an NPN transistor
as a latching switch which is simpler than a conventional flip-flop. [5]
A 1,344 bit memory has been fabricated from 9-bit chips and 16-bit
chips are being investigated. The elements are designed to operate
at very low power levels (e. g., approximately 2 milliwatts per
element). The cost per bit is estimated to be less than $1.00 per
bit by 1967.

The next step beyond the use of multi-stage integrated circuit chips is the fabrication of several hundred bits, or more, of semiconductor storage in a single silicon chip using matrix addressing and selection techniques. This type of active circuit storage utilizing bipolar transistor techniques has been demonstrated in the laboratory with complexity equivalent to 200 gates.[6] A small array of this type providing 4 words of 9 bits each on a single chip (60 x 80 mils) in a 16 lead package has been developed and incorporated in a 256 word 72 bit experimental memory with a 150 nanosecond write cycle time.[7] Such arrays will be utilized for small high-speed control memory or scratch pad applications by 1967. At present, however, the most advanced work is a shift register using metal-oxide semiconductor field-effect type elements. Several companies are also actively working on MOS storage registers of the non-shifting type for control and scratch-pad memories. Similar work is underway on bipolar memory systems.

One semiconductor manufacturer reported work over a year ago on a small low-cost random-access memory array mechanized with MOS elements which was significant in that a single chip contained an order of magnitude more components than other integrated circuits being manufactured at that time.[8] More recently, another manufacturer has produced a 100 bit MOS shift register on a single chip. Because of the high impedance of the MOS, the speed of these devices is relatively slow compared to integrated circuit flip-flops using bipolar transistor techniques, but they are of great interest because the MOS devices are easier to fabricate than epitaxial integrated circuits. Since fewer processing steps are involved, the fabrication of very large arrays of elements with reasonable yields is more feasible, but a speed improvement of an order of magnitude is probably the best that can be expected in this type storage.

As integrated circuit technology and yields improve, the fabrication of somewhat similar arrays of storage elements permitting significantly higher speeds through the use of planar epitaxial transistor elements rather than MOS elements can be expected. Some have predicted that large scale integrated circuit (LSI) arrays utilizing bipolar transistor techniques will eventually replace magnetic core memories in applications where relatively high speed (e. g. , 0. 5 microsecond) is required and where a volatile type memory is acceptable. [9] This prediction implies that high-speed integrated circuit storage arrays of this type can be built with high yields at a cost that will be more than competitive with magnetic core memories. The power required per stage is a serious consideration for any active storage array where holding power is required for each bit position in the array. Very rapid and significant progress is being made at this time in large scale integrated circuit (LSI) technology that will lead to feasible, large, low cost, high reliability semiconductor memories using both MOS and bipolar techniques. This may occur much sooner than is generally expected.

Integrated circuits have been used or proposed for discrete bit storage, registers, scratch-pad memories, [5] main internal memories, [9] and associative memories. [10]

3. 2 Planar Magnetic Thin-Film Memories

Planar magnetic thin-film memories represent one of the longer established approaches to batch fabrication of storage arrays. At present, they are used primarily in small high-speed control and scratch-pad memories but one manufacturer has announced a large scale commercial computer in which the main memory is a 16, 000 word 52-bit thin-film memory with a 500 nanosecond read/ write cycle. [11] This memory uses large thin-film arrays of

1,024 x 208 bits each. Most previous thin-film developments used
a smaller array of discrete elements fabricated by vacuum deposition
processes on a substrate such as glass or aluminum. [12, 13] Each
element is typically about 1,000 angstroms thick and is approximately
25 x 50 mils in area. Some more recent developments use either
a continuous sheet [14, 15] or narrow strips [16, 17] of thin magnetic
film vacuum deposited on the substrate. The X and Y drive lines
are either vacuum deposited on the same substrate with appropriate
insulation between them or, in some cases, the drive lines and
sense lines are fabricated on separate substrates which are then
mechanically superimposed over the one containing the magnetic
elements. Registration problems are less severe for the strip and
the continuous sheet arrays.

Anisotropic material (not isotropic) is used so that there is
a preferred direction (or easy axis) of magnetization. In a
conventional planar thin-film memory, the word lines run parallel to
the easy axis of magnetization creating a field pattern in the hard
direction. The digit and sense lines run parallel to the hard axis
of magnetization creating a field pattern in the easy direction.
A word line rotates all bit positions of a word in the hard direction,
but they tend to flip back when released. A relatively small digit
signal pushes them into the one state or back to the zero state as
desired.

The flux path is not closed; hence, the sense signal is small because
the flux is only rotated rather than switched. This results in a
smaller sense signal and a tendency to creep or demagnetize along
the outer edges of the bit spot. Due to the latter effect, a large
number of disturb signals may tend to destroy the information stored

in the bit position. To alleviate the creep problem, the film is made thinner. The thicker the film, the greater the tendency to demagnetization and creep, but on the other hand, the thinner the film, the less the sense signal. Hence a compromise must be made between the desired sense signal and minimum creep in choosing the thickness of the film.

A number of problems have plagued thin-film memories including dispersion, skew, high drive signals followed by low sense signals, magnetostriction, and yield. Until recently, yields in the order of 30% to 50% in small planes (e.g. 64 x 48 bits) were considered good, but very high yields are being achieved now on planes of this size. However, it is not economically sound to build a large memory out of a multitude of small planes because of the inter-connection and mounting problem. To make an economical large array, it is necessary to fabricate a large plane with a large number of bit positions, but the yield problem becomes worse in this case. As mentioned previously, one manufacturer now makes 1024 x 208 bit planes and has announced a commercial computer using these planes in the main internal memory. They state that yield is no longer a significant problem in thin-film memories. Because of the inherent magnetic properties of planar films, thin-film memories are usually operated in a linear select or word-oriented mode rather than a coincident-current mode. This increases the cost of the associated electronics, but the use of rotational switching permits higher speed operation than in a magnetic core matrix memory.

Since many companies are working on magnetic thin-film memories, it has been predicted that within the next few years they will replace linear select magnetic core matrix memories for high-speed applications. However, of the advanced magnetic memory technologies presently

under development, it is not apparent at this time that planar thin-film memories will be the one that will ultimately succeed in replacing magnetic core memories for main memory and very large capacity applications. High-speed control memory and scratch pad memory applications are the major areas in which planar thin-film memories are currently being used, but integrated circuit memories will take over these applications.

Another possible application area is that of very large-capacity low cost memories,[16,17] but a memory of this type is at least three or four years away. In fact, interest in magnetic thin films for this type of memory seems to have waned recently. The use of thin-films in the intermediate area between 10^5 and perhaps 10^6 bits now appears to be the most promising area for thin-film memories. The fact that thin-film memories now appear more promising for main internal memory applications represents a significant change during the past year.

In small memories, the array cost is negligible, the electronics predominate, and the main advantage is the speed that can be achieved (in the order of 100 nanoseconds or less) that cannot be matched by cores; but integrated circuit memories will dominate this area. In large memories of over 10^6 bits, the array cost begins to exceed the electronics cost and the advantage is in the low array cost; but plated wire and etched-permalloy toroid memories will be more economic in this area. Magnetic core memories will continue to dominate the range from a few hundred words of 1/2 microsecond memory to approximately 100,000 word memories (the range of main internal memories) for some time, but the batch fabrication aspects of thin-film memories and some of the other types discussed later may alter this balance by 1970.

Planar thin-film memories have been designed or proposed for
scratch pad,[12] main internal memory,[11] NDRO,[18] large capacity
auxiliary memory,[17] and aerospace[19] applications.

3.3 Plated Wire Memories

Another type of magnetic film memory is fabricated by plating a
magnetic film on a wire substrate.[20] The wire substrate then serves
as one of the electrical conductors in the system. A closed flux path
can be obtained by using the magnetic film surrounding the wire in a
small region. A cylindrical film of this type offers advantages over
planar films in that the closed flux path and the close physical coupling
between the film and the wire substrate require smaller digit currents
and produce a larger sense signal. Use of the wire substrate as either
the digit or word conductor reduces the mechanical registration
problems in the fabrication of the memory. The major problem with
this type of memory has been the difficulty of producing satisfactory
cylindrical films with high yields. Recent developments in these
fabrication techniques have made this type of memory appear very
promising. A detailed comparison of plated wire and planar film
memories has been presented in a paper by Danylchuk and Perneski[21]
and a comparison of cylindrical and flat film properties in a paper
by Dove, Long, and Schwenker.[22]

In one type of plated wire memory the direction of magnetization
of the cylindrical elements is circumferential to the plated wire providing
a closed flux path. A 10^8 bit solid state mass memory based on this
plated wire technique is being developed under an Air Force contract.[23, 24]
A 10,000 angstrom permalloy film is plated on a 5 mil beryllium copper
wire. This wire acts as both a substrate for the plating and as the
digit drive and sense wire. During the plating process, a polarizing
current is sent down the wire to give a magnetic easy axis circumferential
to the wire. The word drive conductors consist of flat metal straps

placed over the parallel digit wires. The word drive straps are either returned under the digit wires or terminated in a ground plane beneath the digit wires. The digit wires are placed on 15 mil centers and the word drive straps on 45 mil centers. The bit density is approximately 1,500 bits per square inch. This memory uses low-level sense signal switching and selection prior to the sense amplifier. The same two-transistor switching matrix is used for the sense signal and the digit drive signal. Hence, one end of the switching matrix can be connected directly to the berillium copper wire substrates that serve as digit drive lines and sense lines.

Another type of plated wire memory is very similar but uses a weaving process to fabricate the plane. The plated wire, which acts as both the storage media and the digit drive line, is woven into a matrix at right angles to the insulated word drive lines.[25, 26, 27] This provides a tighter magnetic coupling than in the previous approach, but the major differences are in fabrication techniques.

In another type of cylindrical film memory presently used in a commercial computer the direction of magnetization of the cylindrical elements is parallel to the center conductor rather than circumferential to it.[28, 29] In this "rod" memory, a 4,000 angstrom cylindrical film of magnetic material is deposited over a conductive substrate. The axial switching mode produces an open flux path element. A multiple turn winding is placed over the plated rod for each bit position. The plating material is essentially isotropic, and proper operation of the memory does not depend upon anisotropy in the material. Although it is not a true batch-fabrication process, two major factors make the rod memory economically feasible:

Rod manufacture is a continuous process including the automatic winding of spiral wires around the rod

Tooling has been developed to permit automatic fabrication of the memory stack (including multiple turn windings into which the rods are inserted).

The lack of a closed flux path is a disadvantage, but the use of a high coercivity magnetic material, permitted by the tight coupling of the multiple turn winding, overcomes this disadvantage. Fast switching and large output signals can be obtained as a result of the high coercivity of the material, the tight coupling, and the multiple turn windings.

Advantages cited for plated wire memories include low cost, high speed, simple fabrication, closed-flux path possible, and capability for non-destructive read out operation. As a result of these advantages, plated wire memories may win out over planar thin-film memories in most applications, but the relative performance for the fastest scratch-pad applications is more controversial. However, problems have been noticed recently that have been associated with aging of the wire after plating. This appears to be more pronounced at higher temperatures and results in creep between adjacent bit positions. It is believed that this problem will be solved as better plating and handling techniques evolve from present production activities. Certainly, plated wire memories are a major candidate for replacing magnetic core memories within the next three or four years.

Plated wire memories have been designed or proposed for mass memory,[24] internal memory,[29] aerospace memory,[30, 31] read-only memory,[32] and associative memory[33, 34] applications.

3.4 Etched-Permalloy Toroid Memory

The etched permalloy-toroid memory is another promising approach
to the batch fabrication of low-cost large-capacity memories.[35, 36]
In this technique a permalloy sheet is bonded to a substrate, a
pattern is printed on photo resist covering the sheet, and the permalloy
is etched away to leave a matrix of toroidal permalloy storage elements.
Several successive plating, printing, and etching processes are involved
in making the conductors on both sides of the array for the drive and
sense wires and the connections from one side of the array to the other
through the toroids. This approach depends upon plating and etching
techniques rather than vacuum deposition. The storage elements and
all of the drive lines, sense lines, and interconnections are batch
fabricated on the same substrate.

A 10^8 bit solid-state mass memory based on this technique is also
being developed under an Air Force contract.[37] A large capacity
memory is being developed in which coincidence selection is used
to reduce the electronic costs, and in which a very large memory
plane (256 x 256 bits) is used to reduce wiring fabrication costs as
well as drive, selection, and sense electronics costs. This solid-
state mass memory will be made of 6.5 x 10^6 bit modules each
containing 100 of the 256 x 256 planes. The smallest unit that is
handled individually in processing is a matrix plane of 65,000 bits.
The memory has a read/write cycle time of 35 microseconds and
an access time of 15 microseconds. Although this is slow compared
to internal memory speeds, it is very fast compared to conventional
electromechanical mass memories.

Coincident current write and an unusual type of coincidence for
read selection are used in this memory. Coincidence of two RF
frequencies is used in read selection with the sum or difference
frequencies (resulting from the non-linear characteristics of the

magnetic toroid) being detected for sensing. This read technique provides an NDRO memory.

For the 10^8 bit memory, the etched-permalloy toroid approach requires less power (approximately 200 watts), smaller size (4 cubic feet), and less weight (400 pounds) than other solid-state mass memories that are being developed. The closed flux path in the toroid provides a tighter magnetic coupling to the drive and sense lines and minimizes interaction between adjacent bit positions which permits high density. Because of the batch-fabrication processes and interconnection techniques involved, this promises to provide a large capacity memory that will be significantly cheaper than magnetic core mass memories.

This type memory is also attractive for aerospace applications because of the low power, low weight, and small size.[36] The low coercive force for the permalloy toroid permits low drive currents that are compatible with integrated circuit capabilities. Since the toroid provides a closed flux path in which the material is switched in writing and reading, relatively large sense signals are obtained which simplify the sense amplifier requirements. For this application a linear-select mode is used rather than that described above for the mass memory. An aerospace memory of this type is being developed that has a 2 microsecond read/write cycle time for an 8,000 word 30-bit memory requiring only 64 cubic inches of volume and less than 10 watts of power.[36]

The speed capabilities of the etched-permalloy-toroid memory, which are less than those of planar or cylindrical thin-film memories, are not suited to scratch pad and fast internal memory applications. It is promising for applications where low cost or low power, size, and weight are more important than high speed.

Etched-permalloy-toroid memories are being designed for internal memory, mass memory, and aerospace memory applications. [36]

3.5 Monolithic Ferrite Memory

Several development efforts have attempted to batch fabricate memory arrays using ferrite materials. [38, 39] An early example that was manufactured on a production basis was the apertured ferrite plate memory. [40] The monolithic ferrite memory, previously called the laminated ferrite memory, is the only advanced memory of this type that has been carried to production status. [41]

Basically, the monolithic ferrite memory consists of a matrix of X and Y wires imbedded in a solid sheet of ferrite. In fabricating the memory plane, a pattern of parallel conductors is printed on a glass substrate by a silk-screening type process. A film of ferrite is spread over the conductor pattern on the substrate by a process called "doctor-blading." After the ferrite binder dries, the ferrite is peeled off the substrate with the conductors imbedded in the ferrite sheet. This sheet is approximately 0.0025 inches thick. A second ferrite sheet is made with the conductor pattern running at right angles to that in the first sheet. A third ferrite sheet, without imbedded conductors and only 0.0005 inches thick, is inserted between the two ferrite plates with the orthogonal conductors. This three-sheet sandwich is laminated by pressing the sheets together at moderate pressures and temperatures. Sintering the laminated sheets in a controlled temperature furnace provides a uniform isotropic material. The wafer formed in this way in present production is approximately 1 inch square and 6 mils thick providing a 64 x 64 matrix. The conductors are spaced on 15 mil centers.

The matrix of conductors provides the necessary wires for a two wire linear-select memory system in which the wires in the

word oriented direction are used as read and write drive lines and the wires in the perpendicular direction are used as sense lines and digit drive lines. The write current generates a closed flux path in a plane perpendicular to the plane of the read/write drive wire. Simultaneously, the current through the digit wire rotates the magnetic vector slightly, resulting in a component of magnetization perpendicular to the bit/sense wire. The direction of this component is determined by the information to be stored. A subsequent word-oriented read current destroys this component and the resulting $d\phi/dt$ produces the read-out signal. A bit position consists of the crossovers between the word line and two adjacent bit lines; hence, the wafer described previously stores 64 words of 32 bits each.

It is necessary to operate this memory in a word organized manner, but reductions in electronics costs resulting from integrated circuit advances may permit competition with memories that require less electronics. Most of the higher speed advanced memory technologies tend to require linear select operations. The developers of the monolithic ferrite memory believe that the larger number of circuits required in the linear select mode will be off-set by lower costs resulting from less critical tolerance requirements. Significant success in reducing the cost of the memory depends upon the use of relatively cheap integrated circuits to permit the electronics associated with the memory to be made by batch-fabrication processes. The low digit current requirements facilitate the use of integrated circuits. Integrated diode arrays for selection are also planned and integrated stored-charge diodes have been developed which permit steering the bipolar word current pulses with a single diode per word. These are expected to be only slightly more expensive than conventional integrated selection diodes. Fabrication of larger

arrays (e. g. 256 x 256) to reduce the number of interconnections will probably be required for the monolithic ferrite memory to compete economically with some of the other types of advanced memories in large capacity applications. Yield and adequate uniformity between elements may present problems in fabricating arrays of that size.

Monolithic ferrite memories with capacities in the 64 to 4096 word range with cycle times between 0. 5 and 2 microseconds have been reported.[41] However, it is doubtful that this type memory will be a major contender for applications in future naval tactical systems.

Monolithic ferrite memories have been proposed for NDRO, scratch pad,[42] main internal memory,[42] and aerospace applications.

3.6 Magnetic Core Memories

Magnetic core memories consisting of individual discrete magnetic cores threaded by selection, write, and sense wires to form a matrix or storage array have been the best established and most widely used memory technology for over ten years. This type of memory is so well established that its basic principles are well known and have been covered in textbooks.[43, 44]

There are now three major types of core memories. In the first, the selection is accomplished by coincidence of a current in one wire threaded through the core in the X direction and a current in another wire threaded through the same core in the Y direction, each conducting one half the required selection current. In addition, since a number of planes are usually addressed in parallel, a third wire through each core is used to carry one half excitation current in the opposite direction to inhibit those

bit positions in which zeros are to be written when writing a new word in a specified memory location. Hence, coincident current memories are three wire (or 3D) systems if the inhibit wire is also used as a sense line. If a separate sense line is used it then becomes necessary to thread a fourth wire through each core. This tends to increase fabrication costs and the necessary inside diameter of the core.

In the second type, the selection is by a semiconductor or magnetic decoding tree which provides excitation current to all of the bits of the selected word with digit wires carrying inhibit currents through those bit positions of the word in which zeros are to be stored. These linear-select or word - oriented memories are two wire (or 2D) systems. Only two wires are required to be threaded through each core unless a separate sense line is used.

In general, coincident-current core memories are cheaper because of the XY matrix addressing and selection (i. e. , less selection and addressing electronics), but slower because of the tighter tolerances required on drive signals and the limitation necessary on the maximum drive current that can be utilized in each line (i. e. , less than the minimum switching current). Word-oriented core memories, on the other hand, tend to be more expensive because of the linear selection circuitry required, but faster because of the less critical tolerances and the ability to switch the core faster by providing significantly more than the minimum switching current.

The most recent addition to the magnetic core memory family is the 2 1/2 D organization which represents a compromise between coincident current and linear-select memory organizations. Essentially, 2 1/2 D memories use a coincident current read and a linear-select write in which the digit current is additive

rather than subtractive. Furthermore, the word current can be either positive or negative with the phase being used as part of the selection mechanism to reduce the electronics in the word direction. A small selection matrix is used to select one of a number of bit lines for each bit position to reduce the electronics in the bit direction. The 2 1/2 D organization permits using smaller cores since only two wires are threaded through each core, permits faster operation than a coincident current memory and lower cost than a linear select memory, and does not require inhibit recovery time since there is no inhibit current. The maximum length of the drive line is also limited which permits faster rise times on the drive currents and relatively low drive voltages. In one particular 2 1/2 D memory system a 900 nanosecond cycle time was achieved using a 30 mil core which would have required a 20 mil core for a coincident current organization.[45]

The replacement of magnetic cores by other memory technologies has been predicted frequently. However, magnetic core technology is so widespread and well established that it has presented a difficult and rapidly moving target for new technologies. For example, in approximately 1960, the advanced state-of-the-art in magnetic core memories was represented by 4 microseconds cycle time and costs in the order of 25 to 50 cents per bit. By 1962, the speed had increased to 2 microseconds for roughly the same cost and by late 1964 to 1 microsecond for 10 to 15 cents per bit. Today, 700 nanoseconds cycle time large capacity memories (e. g., 64,000 words) are quoted at 7 cents per bit including all associated electronics. Three or four years ago, few would have predicted the 500 nanosecond cycle time core memories now being designed for delivery in commercial computers. This increase in speed and decrease in cost has resulted from two major factors - reduction in

core size from 80 mils OD (50 mils ID) to 12 mils OD (7 mils ID)
and significant advances in semiconductor technology. The latter
has permitted faster and higher power drive and selection circuitry
and lower cost high-gain sense amplifiers.

Magnetic core memories have been used for scratch pad[46, 47],
main internal memory[47, 48, 49], mass memory[50, 51, 52], and
aerospace[53, 54] applications.

3.7 Cryogenic Memories

Cryogenic memories are based on the principle that at temperatures
near absolute zero degrees, the resistance of certain materials
(super-conductors) may be either zero or some finite non-zero
resistance depending upon the magnitude of the magnetic field
surrounding the superconductor.[55] In one type of continuous-sheet
cryogenic memory under development, the storage media is a
superconducting tin film.[56] This tin film, a lead sense line, and
lead drive strips are fabricated by vacuum deposition techniques on
a two-inch square substrate. These metallic films are all insulated
from one another by vacuum deposited insulating films (silicon
monoxide). The sense line is beneath the storage plane and is
oriented diagonally to and directly under the intersections of the
two sets of drive strips which are orthogonal to one another.

Coincidence of the "X" and "Y" drive currents at an intersection
of the drive strips produces a magnetic field sufficiently strong to
switch the region of the storage plane beneath the intersection out
of the superconducting state, thus permitting magnetic flux to link
through the plane in that region. When the currents are removed, the
flux linking the small region of the continuous sheet is trapped,
and persistent currents are established in the storage plane to support
this trapped flux. The stored information can be read by subsequently

applying a coincidence of drive currents of proper polarity, and then sensing the voltage change on the sense line.

A cavity sensing technique is used in one version rather than a zigzag sense line.[57] A second continuous tin film is located a slight distance beneath the storage plane and connected to it electrically along one edge. When the proper polarity drive currents create a magnetic field sufficient to destroy the super-conducting state in the region of the intersection, a change of flux is created beneath the intersection within the cavity between the storage plane and the sense plane. This causes a sense pulse at output tabs connected to the sense plane. Cavity sensing avoids the necessity for accurate registration of the sense line beneath the plane with the intersections of the X and Y drive lines on top of the plane, but some problems have been encountered in obtaining a uniform output signal over the entire plane.

The continuous-sheet cryogenic memory is made by a batch-fabrication process in which a continuous sheet superconducting storage film and sense film and the X and Y drive strips are vacuum deposited for an entire plane. In addition, the X and Y selection is implemented with cryotrons that are vacuum deposited on the same plane and connected to the drive strips by the deposition process. The ability to fabricate the cryotron selection matrix at the same time the storage plane is fabricated is one of the major advantages of cryogenic memory technology.

In one development program, a 16,384 bit memory plane (123 x 128), including 508 cryotrons for XY selection, has been fabricated on a 2" by 2" substrate.[58] Twenty-six vacuum deposition steps using 16 different masks were required. The planar density is approximately 10,000 bits per square inch. Planes of 1024 x 1024 on a 6" x 6" substrate are an eventual goal. Those working on

cryogenic memories anticipate 3 to 5 microsecond cycle times, 10^6 bits in a 10-inch square plane, and 10^9 bits in a complete memory.

Estimates in the order of 1 cent per bit manufacturing cost for 10 million bit cryogenic memories and a fraction of a cent per bit for 100 million bit memories in 3 or 4 years indicate that 10^7 bits is not a competitive size for cryogenic memories and that 10^6 bits is probably the minimum size for which cryogenic technology should be considered. The problems with cryogenic memories are both fundamental and economic. The major technical problem is uniformity. Because of the basic overhead cost in the refrigerant, the cryogenic memory is not a good approach to a small memory, but becomes more advantageous as the size increases. The cryogenic approach may provide a more economic way to reach capacities of 10^9 bits, but other batch-fabrication techniques will be better for capacities of 10^7 bits to 10^8 bits.

The future of cryogenic memories is questionable, but the technology offers some potential advantages.[56, 59] Design and fabrication problems, and rapid advances in other technologies have prevented the cryogenic technology from establishing a foothold.

Cryogenic techniques have been proposed primarily for mass memory[56, 57] and associative memory[60, 61] applications.

3. 8 <u>Serial Memories</u>

This study has concentrated on random access memories since serial memories are not presently a major factor for internal storage functions in general purpose computers. Serial access memories such as mercury delay lines, magnetostrictive delay lines, magnetic drums, and magnetic discs once played a major role as registers and main internal memories. However, as the cost of random access magnetic core memories has dropped and the speed increased, they have tended to completely dominate the

field except for some military and special purpose applications and as secondary storage. Magnetic drums and single disc units with capacities in the order of 200,000 to 10,000,000 bits are widely used as secondary storage and large capacity magnetic drums and multi-disc units dominate the mass memory applications. These large capacity electromechanical auxiliary storage devices are discussed later, but some consideration should be given here to serial internal memories.

As the speed of logical components continues to increase, it may be desirable in some future computers to operate the machine in a bit serial manner with a very high bit rate. For example, this may represent an attractive approach to achieving a very small, light-weight, mobile tactical computer for small Marine Corps units or small ships. In this case, a high-speed bit-serial internal memory would be compatible with the other parts of the machine. If a high-speed bit-serial memory is desired, glass delay lines represent one of the more promising means of mechanizing such a memory. Glass delay lines are similar conceptually to the ultrasonic delay lines used in early computers such as UNIVAC I but provide higher frequencies, larger capacities, and better time and temperature stability.[62]

Typical characteristics for glass memories are:

Average access times	-	5 to 500 microseconds
Bit rates	-	5×10^6 to 20×10^6 bits/second
Capacities (for 100 delay lines)	-	2×10^6 to 5×10^6 bits
Costs	-	2 cents to 50 cents per bit

These characteristics represent a cost performance trade-off between magnetic cores and magnetic drums, but the bit rate of 20,000,000 bits per second is higher than can be readily achieved with other types of memories.

Glass delay line memories usually utilize piezzo-electric input/
output transducers and either a rod of glass (for average
access times below 50 microseconds) or a flat plate of glass
(for average access times above 50 microseconds). In the latter
type, carefully machined surfaces on the glass are used as
reflecting media to permit a multi-path pattern within the
glass plate. This increases the effective length of the delay
line since this is a function of the total path length.

3.9 Magnetic Surface Storage

Magnetic surface recording is used in almost all present on-line
auxiliary storage and off-line auxiliary storage. This technique
has also been used for internal storage in the form of drums
or discs, but magnetic core storage has essentially replaced
these electromechanical devices in most internal memory
applications in the past few years. However, to date there has
been no good replacement for magnetic surface storage recording
in on-line and off-line auxiliary storage. Some of the technologies
discussed previously will eventually replace these devices in
many applications but the timing of this is uncertain. Certainly,
for the next few years, electromechanical devices using magnetic
surface recording will be dominant for auxiliary storage applications.

On-line auxiliary storage, frequently referred to as mass memories,
which are used to provide a large-capacity, fast-semi-random-
access storage are well known and have been described and compared
in a number of previous publications and text books.[63, 64, 65, 66, 67]
They should be under direct on-line control of the computer,
addressable by the computer, eraseable, and reuseable. All
devices of this type that are currently available are electro-
mechanical except for a few large capacity magnetic core memories.
They include large fixed-head drums and discs, moving-head drums,

fixed-head disc files, moving-head disc files, tape loop files, and magnetic card files. The storage media is removable in the tape loop files, the card files, and certain types of disc files to combine a large off-line capacity with a limited capacity on-line random access capability.

All-electronic/magnetic on-line auxiliary storages will be available by 1970 but all of these (with the possible exception of BORAM type devices) will be significantly more expensive in terms of the cost-per-bit for very large capacity storage. This results largely from the fact that the all-electronic/magnetic approaches require addressing each individual word. The electromechanical devices are block-oriented in the sense that access is made to a particular track on a disc, drum or card, and then all information stored in that track (or block) is read or written serially by the same electronic circuitry. Block-oriented random-access memories (BORAM) will provide an all-electronic/magnetic equivalent, if the current development efforts prove successful. [3]

Bit densities of 1,000 bits per inch, track densities of 100 tracks per inch, and bit transfer rates of 1 megacycle are common today for magnetic surface storage. Bit densities of 3,000 bits per inch, track densities of 200 tracks per inch, and bit rates of 2 megacycles are expected to appear by 1967. These figures will probably be doubled by 1970. Capacities of electromechanical on-line auxiliary storage devices range from 2×10^5 to 2×10^9 bits at present. Capacities will probably increase by an order of magnitude within the next few years.

The cost per unit can be expected to decrease even with the larger capacities as the technology is improved and more manufacturing experience is obtained. Hence, the cost per bit of storage

can also be expected to decrease by one to two orders of magnitude--
possibly to 0.0005 cents per bit for the mass memory itself (not
including control and buffering electronics). Although the picture
for the future of capacity and cost appear bright, there is little
hope for significant improvements in average access times for
moving-media mass memories. Due to the inherent mechanical
motions involved, improvements of as much as an order of
magnitude over available devices cannot be expected. Access
times are presently in the order of 15 milliseconds for fixed-head
discs and large drums, and less than 100 milliseconds for many
moving-head disc files and drums. The access times are not
expected to improve significantly for these types of devices--
probably by a factor of 2 at the most. For significant improvements
in access time, solid-state devices will be required.

3.10 BORAM Devices

Several block-oriented-random-access memory (BORAM)
developments are being sponsored by the U.S. Army Engineering
Research and Development Laboratory at Fort Monmouth,
New Jersey.[68, 69, 70, 71, 72]

Although these are batch-fabricated memory approaches, they
differ from those described previously in that they are not random-
access memories. They are block oriented with random access
to the beginning of a block but serial access to information within
the block. A batch-fabricated solid-state memory of this type
could be a replacement for large magnetic drums, magnetic disc
files, and possibly magnetic tape.

Previous types of delay line memories were volatile and suffered
from the large amount of electronics necessitated by the requirement
for regenerating and recirculating the information in each individual
delay line. The necessity for recirculating the information results

in the loss of stored information if power is interrupted. The requirement for electronic circuitry to be in continuous use for each individual line implies a severe cost penalty in very large capacity memories. BORAM approaches require static storage of information without continuous recirculation which, in turn, permits the electronic read and write circuitry to be switched from one line to another as part of the addressing and selection process.

The goals of the Army development programs are to provide a block-oriented-random-access memory with the following characteristics:

1. All electronic
2. Removable media
3. Non-volatile shelf storage of the media
4. Small media size ($<$200 cubic inches)
5. Low media cost ($<$\$500)
6. Media capacity equal to tape (4×10^6 characters)
7. Random access to the block (1 microsecond)
8. Inherent sequential transfer within the block (read-strobe to 1.5 - 3 million characters per second)
9. Read-write unit -

   1/10 the power of tape unit

   1/10 the weight of tape unit

   1/2 the size of tape unit

The success of these development programs will be of great significance to future computer systems. At present, there is no economic all electronic/magnetic replacement for large capacity electromechanical storage devices such as magnetic disc files, magnetic-card memories, and magnetic tape units. Such a replacement will be essential to future systems if the speed, cost, reliability. and size limitations of electromechanical

input/output and auxiliary storage equipments are to be avoided for very large capacity storage functions (now handled by devices such as disc files and magnetic tapes).

Success of the Army programs will offer the following advantages:

1. Static storage
2. Semi-serial access not requiring a physical coincidence of selection wires for each bit position
3. Ability to switch read and write mechanisms from one line to another
4. Large capacity semi-random access bulk storage with no mechanically moving parts
5. Possibility of off-line storage by plugging alternate blocks of delay lines into a read/write device
6. . Low cost per bit of storage

A future all electronic magnetic tape replacement will amost certainly be a block-oriented rather than a random-access-type storage device. A large-capacity, random-access, mass memory offers certain unique advantages, but it is very unlikely that such a device can compete on a cost per bit basis with semi-serial electromechanical devices. The requirement for the physical intersection of electrical signal lines for each bit position and the access electronics will not permit on-line storage costs of a few millicents per bit by 1975. A semi-serial or block-oriented device providing random access to a block of information, but serial access within the block, will be necessary to permit the read/write electronics to be time shared by a serial bit train.

4 ANTICIPATED PERFORMANCE AND COST OF FUTURE MEMORIES

In evaluating and comparing different types of memories, a large
number of characteristics and parameters can be considered. However,
the actual selection of a specific type of memory for use in a
particular function in a new system is usually made on the basis of
only a few of these. The major parameters and characteristics of
concern in selecting the proper storage devices for use in future
naval tactical systems are:

> Type of storage
>
> Storage capacity
>
> Type of access
>
> Access time
>
> Read/write cycle time
>
> Read/write rate
>
> Cost
>
> Availability

Any storage device that does not meet the criteria of high reliability
should be eliminated from further consideration. For some types
of application, additional characteristics such as environmental
capability, size, weight, and power requirements become very
important. The characteristics available in 1966 for storage devices
that are typical of the major categories shown in Table B-1
provide a basis for comparing present technology with that anticipated
for the future. Tables B-2, B-3, and B-4 compare estimates of
the characteristics anticipated by 1970 for high-speed control and
scratch pad memories, main high-speed internal memories, and
solid-state on-line auxiliary storage devices. Table B-5 compares
the characteristics anticipated for electromechanical auxiliary
storage devices using magnetic surface recording.

Type of Storage	Typical Capacity (Bits x 10^3)	R/W Cycle Time (n sec)	R/W Rate (mc)	Vola- tile	Possible Date of First Prod.	Batch Fabri- cated
Monolithic Int. Ckt. Arrays	12	50	20	Yes	1968	Yes
MOS Arrays	50	150	7	Yes	1967	Yes
Planar Thin-Film	25	75	13	No	1966	Yes
Plated Wire	50	100	10	No	1966	Yes[1]
Monolithic Ferrite	25	150	7	No	1967	Yes
Magnetic Core Matrix	50	300	3	No	1966	No

Note: (1) Although the plating of the wire is a continuous process as it passes through the plating path, plated wire memories are considered to be batch fabricated in contrast to memories using discrete elements such as magnetic cores.

TABLE B-2

ESTIMATE OF CHARACTERISTICS OF
HIGH-SPEED CONTROL AND SCRATCH PAD MEMORIES

Type of Storage	Typical Capacity (Bits x 10^6)	R/W Cycle Time (u sec)	R/W Rate (mc)	Vola- tile	Possible Date of 1st Prod.	Batch Fabri- cated
Monolithic Int. Ckt. Arrays	0.4	0.2	5.0	Yes	1969	Yes
MOS Arrays	0.8	0.6	1.7	Yes	1968	Yes
Planar Thin-Film	3.0	0.2	5.0	No	1967	Yes
Plated Wire	6.0	0.3	3.3	No	1968	Yes[1]
Monolithic Ferrite	3.0	0.5	2.0	No	1968	Yes
Etched- Permalloy Toroid	6.0	1.3	0.8	No	1968	Yes
Magnetic Core Matrix	3.0	0.5	2.0	No	1966	No

Note: (1) Although the plating of the wire is a continuous
process as it passes through the plating bath,
plated wire memories are considered to be
batch fabricated in contrast to memories using
discrete elements such as magnetic cores.

TABLE B-3

ESTIMATE OF CHARACTERISTICS OF
MAIN HIGH-SPEED INTERNAL MEMORIES
BY 1970

Type of Storage	Typical Capacity (Bits x 10^8)	R/W Cycle Time (u sec)	R/W Rate (mc)	Vola-tile	Possible Date of 1st Prod.	Batch Fabri-cated
Planar Thin-Film	1	1	1	No	1969	Yes
Plated Wire	2	1	1	No	1968	Yes[1]
Etched-Permalloy Toroid	2	35	0.03	No	1968	Yes
Magnetic Core Matrix	1	3	0.33	No	1966	No
Continuous Sheet Cryogenic	10[2]	5	0.2	No[3]	1970	Yes

Note: (1) Although the plating of the wire is a continuous process as it passes through the plating bath, plated wire memories are considered to be batch fabricated in contrast to memories using discrete elements such as magnetic cores.

(2) Technical problems that have been encountered raise some question as to whether cryogenic memories will prove feasible, but if they do, capacities of at least an order of magnitude greater than shown in this table could be realized in the early 1970's.

(3) Cryogenic memories are not volatile in the conventional sense but stored information will be destroyed if power remains off of the refrigerator long enough for it to warm above the superconductor temperature.

TABLE B-4

ESTIMATE OF CHARACTERISTICS OF
SOLID STATE ON LINE AUXILIARY STORAGE BY 1970

Type of Device	Capacity Per Unit In Bits x 10^9	Average Access Time	Track Transfer Rate Bits/Sec x 10^6	On-Line or Off-Line Storage
Moving-Head Magnetic Drums	2	60 ms	2	On-Line
Fixed-Head Disc Files	1	15 ms	3	On-Line
Moving-Head Disc Files	10	60 ms	2	On-Line
Removable Disc Files	0.5	80 ms	2	Either
Magnetic Tape Loop	0.2	80 ms	0.4	Either
Magnetic Tape Reel	0.5	(serial)	0.4	Off-Line
Magnetic Card Files	10	200 ms	0.7	Either

TABLE B-5

ESTIMATE OF CHARACTERISTICS OF
ELECTROMECHANICAL AUXILIARY STORAGE
BY 1970

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The comparisons given in these Tables show characteristics that are expected to be typical for each memory technology, but they do not represent the extremes in either direction. These characteristics are believed to be achievable, but whether they are actually realized depends upon the extent to which their development and production is supported. The best technique does not always win.

The following explanations and comments should be kept in mind when considering the comparisons in these Tables:

Typical Capacity - The typical capacities shown do not necessarily imply a single module of that capacity - particularly for the larger memories. In most cases, the typical capacity is determined more by the requirements of the systems' designers than by limits of the technology. For example, in comparing main high-speed internal memories, capacities in the order of 3 million bits are shown for most of the storage types. Capacities of 6 million bits are shown for the etched-permalloy-toroid and plated-wire memories because larger capacities may be somewhat easier to achieve with these technologies - not because the other technologies are incapable of providing that capacity. In all cases, 3 to 6 million bit memories would probably be made in several modules.

Read/Write Cycle Time and Read/Write Rate - The numbers shown in these columns represent the rates at which the devices are expected to operate in the particular category and type application. Faster rates are usually possible for smaller capacities or higher costs.

Possible Date of First Production - This column requires careful interpretation. Based on the state of research and development in the individual technologies, it is believed that

memories of these types could be put into production in the years shown if sufficient incentive exists for doing so. Actual operational use in naval tactical systems will probably lag these dates by at least two years because of system design and field test requirements. However, the characteristics indicated are estimates of those expected to be typical of each type memory in 1970, but these may not appear in operational military systems until approximately 1972. Slower speeds or smaller capacities may be available sooner. Some of the memory types, of course, are already in production but with lesser characteristics. In some cases, these possible production dates may not be met simply because only one or two companies are working on the specific technology and they may not schedule sufficient efforts and expenditures to meet dates that are technically possible. The availability of government support is also an important factor in determining whether these possible dates are met. Some of the dates, of course, may not be met because of technical problems that prove to be more difficult than is presently anticipated.

Once reliable memory technologies have been isolated that meet the performance and operational requirements of the application, cost ultimately becomes the deciding factor. Although established technologies, such as magnetic core memories, have a decided advantage in the short run, they will ultimately yield to batch fabrication technologies. When technical and manufacturing feasibility is proven, batch fabricated devices will prove superior with respect to cost and reliability to those fabricated from discrete components. The cost is primarily a function of three things:

1. The number and type of processing steps involved
2. The number of bits of storage fabricated in a single set of processing steps
3. The yield

The last is extremely important since there are several memory batch-fabrication technologies that are feasible today but whose yield is too low to permit them to compete economically. To a large extent, the yield depends upon understanding the chemical and physical processes involved and developing techniques for adequately controlling the processing steps.

In memory technology, two types of batch fabrication must be considered:

> Batch fabrication of the storage array; and
> Batch fabrication of the reading, writing, and addressing electronics.

Most of the technical discussions in this paper have dealt with array fabrication, but the reading, writing, and addressing electronics will benefit from the rapid progress in integrated circuit technologies. To a certain extent, these techniques are similar for many of the memory technologies. Integrated sense amplifiers are already available. Write drivers for some of the types of memory are available and selection matrix segments are being developed.

For small memories, the electronics costs predominate, and for large memories, the storage array costs predominate. Hence, registers and high-speed control and scratch pad memories will benefit most from integrated circuit advances, while large capacity on-line auxiliary storage will benefit most from batch-fabricated array developments. For main high-speed internal memories, the two are more evenly balanced and improvements in both are required if costs are to be reduced significantly.

It is very difficult to predict future production costs for specific memories that are presently under development in the laboratory. Also, the costs of storage will vary with speed and capacity and the

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particular technique employed. However, typical costs for given categories of storage can be forecast with reasonable confidence that one or more of the possible technologies will meet the forecast. Typical memory costs anticipated by 1970, including the storage media and all mechanical and electronic components necessary to provide an operating memory are:

> Registers and high-speed control memory - 2 to 5¢ per bit
>
> Main internal memory - 1 to 3¢ per bit
>
> Solid-state random access on-line auxiliary storage - 0.2 to 1¢ per bit
>
> Electromechanical on-line auxiliary storage - 0.001 to 0.01¢ per bit

The costs shown above compare with present costs of 50¢ to $10 per bit for registers and high-speed control or scratch pad memories, 5 to 50¢ per bit for main internal memories, and 0.01 to 0.2¢ per bit for electromechanical on-line auxiliary storage. The cost figures used here are commercial prices that a memory supplier would quote to a computer manufacturer for production quantities; hence, they represent more than bare manufacturing costs. However, requirements for meeting military specifications such as MIL-E-16400 may increase these anticipated costs by approximately 50%.

Although it is difficult to predict production costs for future memories that are presently under laboratory development, estimates can be made of the techniques that are most likely to be lowest cost based on the fabrication processes involved. Storage hierarchies for future computer systems based on minimum costs will probably consist of the following:

Discrete bit storage and registers	- monolithic integrated circuits
Smaller high-speed control or scratch pad memories	- monolithic integrated circuits
Larger high-speed control or scratch pad memories	- MOS arrays
Main internal memories	- plated wire
Solid-state on-line auxiliary storage	- etched-permalloy toroid
Electromechanical auxiliary on-line storage	- magnetic card files
Off-line auxiliary storage	- magnetic tape

The need for higher performance characteristics will frequently dictate the choice of other types of storage in most of these categories. The listing above is based entirely on minimum cost and does not reflect performance nor cost-performance trade-offs.

It is difficult to place ultimate limits on the cost, speed, and capacity of different memory types since the violation of basic physical laws has not been the limiting factor to date and probably will not be for the foreseeable future. The comparisons given in Tables B-2, B-3, B-4, and B-5 indicate the characteristics anticipated for a 1970 era system but these are not ultimate limitations in most cases. It is important to note that in considering the limitations, the set of characteristics must be taken as a whole. For example, for a particular type of memory, a certain combination of speed and cost may be anticipated for a 1970 era system. However, if the capacity were decreased significantly, the speed could be increased. Therefore, the characteristics shown in these tables should not be considered as limitations on any individual characteristics, but rather as a reasonable expectation for combinations of characteristics for 1970 to 1975 systems.

A number of memory experts have given consideration to ultimate limitations of memory technologies and future characteristics have been predicted in previous surveys. [1, 2, 42, 63, 65, 66, 73, 74, 75]

5 SYSTEM IMPLICATIONS OF ADVANCED MEMORY TECHNOLOGY

The cost and performance characteristics of the advanced memory technologies discussed here will have profound effects on the future design and use of computer systems. Machine organization, programming techniques, system organization, and computer users will all be influenced by increased speed and capacity and lower costs.

5.1 Machine Organization

Although memory speeds will increase significantly, storage functions will still be slow compared to logic functions. The utilization of very fast scratch pad memories of several hundred words capacity and of very large capacity main internal memories can partially compensate for this in terms of the effect on systems speed. The decreasing cost of electronics associated with memory arrays will permit overlapping a number of banks of memory economically to achieve higher effective speeds. Larger capacities at each level of the storage hierarchy will minimize the number of accesses required to the next higher (and slower) level. For example, as the cost of high-speed scratch-pad memories are reduced sharply, it will be feasible to utilize larger capacity scratch pads which will permit storing more data on instructions in the fast scratch pad memory so that fewer accesses are required to the slower main internal memory.

Faster speeds, lower cost, and more efficient accessing techniques will permit a truly memory-centered processor. Integrated circuit registers and scratch-pad memories will permit the use of a large number of high speed registers. Hence, it will be feasible and economic to have a relatively large number of multiple index registers, arithmetic registers, and control registers. These may be implemented as general registers in a high-speed control memory where a given memory location can serve as an index register, an arithmetic register, a control register, or a high-speed data or instruction storage location. The use of flexible high-speed general registers will significantly reduce the time required for "red tape" or "housekeeping" type operations.

If hierarchial memories are to be used efficiently, improved machine organization techniques for making the entire internal and on-line auxiliary storage appear as a single uniform storage to the user will be necessary. This may require a combination of machine organization and software techniques. New types of memories may also permit implementing new machine languages that will facilitate and simplify the compiling operation by providing a machine language that can be more easily related to the programmers' pseudo-language.

5.2 Programming

Large-capacity low-cost storage will permit storing larger programs. With larger program storage, subroutines can be stored in the proper forms and appropriate locations in the main program rather than requiring reference to standardized subroutines by transfer-of-control instructions. Many alternate programs and the major part of the systems software or compiler and subroutine libraries can be stored either in the main internal memory or in high-speed random-access on-line auxiliary storage. The availability of large capacity storage that is cheap enough to be used inefficiently will also permit storing large tables and other types of constants and data rather than recalculating them every time they are to be used.

Programming will become easier since it will not be as important to write efficient programs in terms of the number of instructions required and because of the reduction in the number of "red tape" operations as a result of the availability of large numbers of high-speed general registers or multiple index, arithmetic, and control registers. The ability to tolerate programs that are inefficient in terms of the number of instructions required will also simplify programming languages.

System Organization

From the overall system standpoint, one of the major problems facing those planning future naval tactical systems is the increasing imbalance between central processors and internal memories on the one hand, and peripheral and input/output equipment on the other hand. As internal logic and memory becomes cheaper, faster, smaller, and more reliable at a rapid rate, input/output and other peripheral equipment is improving at a relatively slow rate because of the electromechanical nature of most present equipment of this type. Fortunately, lower cost and larger capacity memories can partially compensate for this in several ways:

(1)   Large capacity internal memories can be used to retain data and alternate programs internally rather than dumping them into on-line or off-line auxiliary storage for later recall.

(2)   Low cost storage and buffers can be used to eliminate or minimize certain types of intermediate input/output operations. For example, multiple keyboards can be operated directly into a buffer storage or fast main memory to avoid intermediate punched card or magnetic tape operations. In a similar way, multiple printers, displays, or read-out devices can be operated directly from main memory or a buffer. The requirement for electromechanical input/output and peripheral equipments will be reduced as systems operate on-line to a greater extent with data captured at the source and dispatched directly to the destination.

(3)   Solid-state on-line auxiliary storage can replace some of the electromechanical auxiliary storage devices-- particularly for data and programs where fast access is

advantageous and extremely large volumes of data or instructions are not involved. This type of solid-state storage will fill a gap between internal memories and very large capacity electromechanical auxiliary storage.

(4) Block-oriented-random-access memories (BORAM) will eventually further reduce the requirements for electromechanical on-line auxiliary storage and may eventually permit replacing a large portion of off-line storage, such as magnetic tapes, with removable media BORAM. The BORAM concept will have a significant effect on the organization and use of future systems if current development efforts prove successful.[3] BORAM devices will at least provide another level in the hierarchy of storage and may at best largely replace one or two of the present levels.

Moderately priced fast memories will greatly enhance the systems capability for simultaneously processing multiple input/output channels without interference or interaction. For large scale systems, simultaneous handling of a large number of input/output devices will be essential to avoid seriously limiting the system capability as a result of the speed limitations of the electromechanical input/output equipment.

If future naval tactical systems use time-sharing concepts, their design will be heavily dependent upon the availability of large capacity memories to permit handling alternate programs for multiple users. Improved secondary memories will facilitate present approaches to time-sharing systems in which some users are dumped onto disc file storage while other users are being processed, but very large capacity low cost internal memories may permit maintaining these users in internal storage. They will at least permit processing all users directly from a random-access, large-capacity, solid-state secondary storage with a

resulting savings in time and executive program requirements. However, very low-cost storage coupled with very low-cost logic may have a somewhat opposite effect on systems organization of future time-sharing systems by permitting each user to have a relatively capable, low-cost, individual computer which makes access to the central system only for necessary data, programs, or unusual operations. [76]

Navy Users

Significant reductions in costs of all types of storage, coupled with corresponding decreases in the cost of logic elements, will make low-cost computers available for naval applications where the use of computers has not been considered seriously before for economic reasons. Many new users will be found in smaller ships and for small Marine Corps mobile tactical units. As indicated under the discussion of the effect on systems organization, advances in memory technology will greatly accelerate the trend toward greater on-line use of computers.

The ability to provide solid-state replacements for electromechanical auxiliary storage and some input/output functions will provide major improvements in reliability and maintainability and reductions in size, weight, and power requirements. This will make the use of computers feasible in many military applications where stringent requirements for reliability, maintainability, portability, and adverse operating environments have previously limited their use.

6 PROBLEM AREAS

Detailed consideration of technical problems involved in the design
and fabrication of different types of memories that have been discussed
is not within the scope of this study. However, consideration should be
given from a systems standpoint to a number of problems in the selection,
utilization, and application of memory capabilities that will be available
within the next few years. One of these, the system imbalance
resulting from the failure of improvements in large capacity electro-
mechanical memories to keep pace with improvements in central
processors and internal memories, has already been mentioned.

There are a number of other problem areas that deserve serious
consideration by memory designers, computer designers, Navy
systems planners, programmers, and users. These include:

> Techniques for utilizing batch-fabricated memories
> which contain a limited number of bad elements;

> Improved techniques for sharing the use of large
> memories in large multi-computer systems;

> Systems concepts for minimizing input/output
> operations by using more internal storage;

> Improved concepts of memory utilization in time-
> sharing systems;

> Better understanding of ways to utilize random-access,
> solid-state, on-line auxiliary memories to provide
> another level in the storage hierarchy between internal
> memories and very large capacity electromechanical
>   auxiliary storage;

> Concepts for more effective utilization of high-speed
> control and scratch-pad memories from both the
> machine organization and the programming standpoint;

Better techniques for effectively utilizing large memory words in the order of several hundred bits per word;

Development of low-cost display memories that are integral to the display panel;

Improved modularity in memory design;

Better techniques for implementing large-capacity low-cost serial BORAM type memories;

Techniques for implementing very, very large capacity auxiliary storage in the order of 10^{12} to 10^{15} bits that is accessible by the computer;

Machine organization and software techniques to make storage hierarchies with many levels appear as a single level storage to the user;

Techniques for protecting the data base in multi-computer, multi-user systems with many remote users;

Better understanding of the trade-offs, applications, and organization of multi-level storage hierarchies for specific types of applications;

Techniques for implementing larger capacity solid-state auxiliary storage to meet mobile military requirements for ruggedness, portability, and maintainability under adverse operating conditions.

There are also many problems involved in the proper implementation and utilization of other memory types, such as read-only memories and associative memories, that have not been considered in detail here.

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Appendix C
DISPLAY TECHNOLOGY

1 GENERAL

Future naval tactical systems will require a number of different means
for displaying computer generated or computer processed tactical
information to both operating and command personnel. In a broad
sense, displays can interact with all of the five senses--touch, smell,
taste, hearing, sight. Sound displays in the form of voice output are
discussed in Appendix D with input/output equipment. Other types of
sound displays, such as bells or other audible warnings, which are
easily within the present state of the art, have not been covered by
this study. Tactile displays may be used for specialized purposes in
future systems, but no specific applications or requirements existed
to justify their coverage during the study. Hence, this investigation
of display technology concentrated on visual displays and, more
specifically, on those which are normally expected to be viewed as
the data is presented, i.e., real-time or "near-time-displays"

Hard copy devices, such as printers which may sometimes be used
functionally as displays, were not considered in that category for
the purposes of this study. Printers have been considered input/
output devices and are covered in Appendix D. Simple discrete
character or special word displays that can be implemented with
shaped lights or other existing types of character displays have also
been omitted from serious consideration. This study has concentrated
on two major categories of displays--console displays for use by an
individual or a limited number of users and large-screen displays for
group use.

This appendix discusses technical developments affecting console and large-screen display applications requiring real-time or "near-real-time" presentation of dynamic data which may be changing rapidly. It evaluates the future characteristics anticipated for each of the major display technologies presently in development that appear to be likely contenders for use in naval tactical systems in the 1970-80 era. Most of the display technology discussed here was previously covered in the material prepared in 1964 for the ANTACCS final report, but this appendix reflects the results of the continuing research and development efforts in these technologies during the past two years. Several display technologies that have not proven out have been dropped from consideration. Some of the display technologies covered only lightly in that report have taken on added importance during the past two years. Several new displays techniques have been proposed, but none have proven sufficiently promising to justify serious consideration for use in 1970 era tactical systems. Although some of them may prove feasible for use in the 1975-1980 period, the evidence of their feasibility is not sufficient at this time.

The primary requirement for new display technologies is in the large-screen display area since existing cathode-ray tube technologies are adequate for console type displays. Present CRT type displays are capable of meeting requirements of shipboard operation as well as performance requirements for future naval tactical systems. In many specific CRT display consoles adequate brightness is not achieved under normal ambient lighting conditions, but this is usually a result of equipment design, refreshing techniques, and refreshing rate rather than the inherent brightness capability of the CRT. This is particularly true with display consoles that use a TV raster or PPI scan technique. Although present cathode-ray tube technology is capable of providing the

operational and performance characteristics necessary for future naval
tactical systems, it has several disadvantages that can be overcome in
future systems by the use of new display technologies. These include
the physical size and weight, requirements for high voltage and high
power, inherent analog addressing, lack of inherent long term storage
(thus requiring high refresh rates), and susceptibility to high shock
and high vibration environments. These disadvantages can be overcome
in future console displays by the use of flat-panel display technologies
that are compatible with integrated circuit semiconductor technologies.
Hence, in addition to making feasible real-time, dynamic, large-screen
displays, some of the display technologies discussed in this appendix
also offer potential for reducing the size, weight, and power requirements
of console displays for future naval tactical systems.

The term "display technology" as used in this study has been restricted
to the presentation or generation of the actual visual image--i. e. , the
visual transducer. Character generation, buffer storage, logic and
control, and other electronic or magnetic circuits necessary in a
complete display system are not included in "display technology"
here. Semiconductor circuits and magnetic storage elements are
being used satisfactorily now to implement these latter functions in
new display equipments, but the visual transducer remains a major
problem. Integrated circuit techniques, which are discussed in detail
in Appendix A, are most effective for implementing low voltage, low
power, low precision components. These are ideally suited to the
fabrication of bi-valued computer logic and storage elements, but
unfortunately they are very poorly suited to the implementation of
visual transducers by most of the approaches in use today.

Some of the advanced display technologies discussed in this appendix
offer promise for a flat-panel display that will require significantly less

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physical space than cathode-ray tube consoles and that will be compatible
with the voltage, current and power capabilities of semiconductor integrated
circuits and batch-fabricated memory components. The problems are much
more severe with respect to technologies for implementing large-screen
dynamic displays. The techniques used in present large-screen displays
are not well suited to mobile tactical display systems that must present
dynamic, real-time, graphical data with associated alphanumeric
characters and symbols as well as status information and tabular alpha-
numeric data. Most of these are unsatisfactory from the standpoint
of both real-time dynamic performance and the ability to meet
operational requirements for mobility, reliability, ruggedness,
maintainability, and adverse environmental conditions. This is
particularly true with respect to the mechanical and photographic
aspects of film-based projection systems, mechanical inscriber
systems, and the type of light valves in use at present. Large-screen
displays are needed that can present the same type of data presently
handled by console displays and with essentially the same response
time. Display technologies that do not require large quantities of
non-reuseable media, such as conventional photographic film, are
more desirable for tactical systems.

A multi-color capability is desirable in some display applications, but
the technologies that are well suited for multi-color displays (e. g.
photographic film) are not generally satisfactory from the standpoint
of performance and operational characteristics. Multi-color displays are
possible with some of the promising future large-screen technologies,
but they will require a considerable amount of additional hardware
(e. g. , triplicating the basic visual transducer) will increase
maintenance and logistics problems, and may impair reliability.
Hence, it may be necessary to sacrifice multi-color capability for

tactical displays in favor of simpler equipment with easier maintain-
ability, simplified logistics, and higher reliability. It is difficult to
justify a need for multi-color capability for real-time dynamic displays
for tactical operations in view of the compromises that must be made
to achieve it, but a somewhat better case can be made for multi-color
in large-screen displays than in consoles.

The usefulness of a large-screen or console display depends upon
many factors other than the capabilities of the visual transducer. The
effectiveness of the display depends also upon the method of interfacing
with the computer, the software for controlling the display, the human
factors design, the operator or user functions and controls implemented
in the display, the identification and selection of data to be displayed,
and the overall systems concept. Successful utilization of new display
technologies depends upon equipment and systems design as well as
the characteristics of the visual transducer.

2 TYPES OF DISPLAYS

Displays can be categorized in several different ways but the most convenient categorization for this discussion is one based on a combination of functional and equipment considerations.[1,2,3] On this basis, the three major categories are:

> Indicators and discrete character or symbol displays
>
> Individual or console displays
>
> Group or large-screen displays

In general, the use and mechanization of display equipments for these three categories are different, but there is some overlap of the basic technologies applicable. For example, a cathode-ray tube is good for a console display but is not suitable for a large-screen display. On the other hand, an electroluminescent matrix display may be applicable for either a console or a large-screen display depending upon its size.

Indicators and Character Displays

Limited amounts of information can frequently be handled more easily by indicators or discrete character displays than by an image or multi-symbol display such as a CRT. Examples of displays of this type range from warning lights or status indicators to decimal or alphanumeric displays with groups of digits or characters. Frequently, several sets of numbers or words may be represented by different groups of decimal or alphanumeric indicators, but if very many numbers or words are to be represented in this manner it is sometimes simpler or more economic to provide a CRT which can simultaneously display all of the numbers or words. In this sense the dividing line between choosing discrete character displays or a small console display is flexible. A small console can be mechanized with discrete character displays, but if the amount of information to be displayed is large a

different implementation such as a CRT is usually more desirable. Display devices in this category include lights, electromechanical indicators, electroluminescent characters, nixie tubes, and small lamps projecting light in the shape of a single character on a small screen. Since such devices, also called digital read-outs, are relatively simple and have been discussed in detail elsewhere, they are not discussed further here. [4]

Individual or Console Displays

Size is the major distinguishing factor between console displays and large-screen displays, but the mechanization is significantly different in many cases. The individual or console display is intended for a single user, or at most a limited number of users (e. g. , two or three). Hence, the physical size of the viewing screen usually need be no more than 20 or 25 inches across. Since this size can be handled by relatively conventional cathode-ray tubes, they represent the dominant technology for implementation of the visual transducer in console displays. However, some of the technologies discussed later as being applicable to large-screen displays can and have been used for console displays also. The fact that the CRT is a well-established, well-understood, and economic technology has made it dominant in the console display category, but several disadvantages are discussed later that will lead to its ultimate replacement by new technologies.

Console displays usually include the visual transducer (e. g. CRT), one or more input means (e. g. , a keyboard), and the necessary control functions to permit the user to control the display and communicate his needs to the computer. Hence, most individual displays are relatively complete man-machine consoles, but some individual displays may be essentially monitor devices that display information to the user but permit him little control over it. Many individual console displays are little more

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than alphanumeric inquiry and response devices, while others permit
the display and entry of complex graphical information as well as
alphanumeric data. Console displays are not only the largest but also
the most rapidly growing category of displays because of the important
link they provide in putting the individual user on-line with large computers.
Such displays are essential to facilitate man-machine interaction.

Group or Large-Screen Displays

Large-screen displays are used where it is necessary for a group of
people to view the same information simultaneously. The high cost of
large-screen displays plus the lack of really adequate technologies
for presenting dynamic information on a large screen have seriously
restricted the use of group displays. Significant technological
improvements are necessary to permit satisfactory group displays at
a reasonable price. Most group displays that have been installed to
date involve projection systems of one type or another with the display
generated in one device and then projected onto a screen. However,
work is underway on several technologies that will permit the generation
of the visual image in the screen itself. Some of these are considered
later in the discussion of display technologies. Most of the research
and development work on the visual transducer portion of display
systems is devoted to techniques applicable to large-screen displays
because of the lack of suitable means for implementing displays of
this type at present. The CRT enjoys a dominant position in console
displays, but there is no equivalent dominant technology for large-
screen displays.

There is some question as to whether the need for large-screen displays
is a real one or is primarily psychological. A good argument can be
made that a group of users each viewing his own individual console with

suitable means for communication (both oral and visual) can provide the same capability as a large-screen display. The functions performed with a large-screen display can also be performed with a system in which each user has an individual console on which he sees the same display as other users, if he has a suitable means for indicating a point or object to the other viewers on their consoles. For example, a light pen can be used as a pointer to cause a blinking circle to appear on the other users' screens similar to the method used in present NTDS displays.

Displays can also be categorized by whether they are alphanumeric or graphical, whether they are static or dynamic, or whether the image is generated by a TV raster scan, by a matrix in which individual points are addressed digitally, or by tracing symbols and vectors in an analog fashion. Another method of categorizing displays is based upon the way light is used to create the visual image-reflective, transmissive, or self generating. Finally, displays can be categorized by their characteristics (e. g. , color) or the technology or hardware mechanization used.

In general, display applications indicate a need for at least three classes of display consoles. The first is a high usage application in which the user is actively solving the problem with the console in a way that may involve frequent changing, transposition, or rotation of alphanumeric or graphical data and frequent instructions, to the computer to change the process of computation or the information displayed. Present and future naval tactical systems require consoles of this type. This type of console may eventually involve a small-scale computer in the console. The second class is a somewhat cheaper console with only alphanumeric capability

but one that still involves a high usage rate. Information storage and retrieval systems and message editing and composing systems require such displays. Applications for consoles of this type are anticipated in future naval tactical systems. The third class is the low cost display used as a remote terminal for systems which are servicing many remote users. In this type of display the usage rate may be relatively low hence low cost is very important. Some remote displays may also require graphical capability. In order to minimize the need for storing digital information to refresh the display at the remote terminal, some form of display screen with an inherent storage capability is desirable for this type of application. These simplified remote terminals will be required in some future naval applications, but their use in tactical systems is not certain at this time.

The most likely contenders for implementing console and large-screen displays in future naval tactical systems are: .

Console displays

Cathode-ray tubes

Photochromic-CRT displays

Electroluminescent matrices

Opto-magnetic matrices

Injection-electroluminescence matrices

Large-screen displays

Photochromic-CRT displays

Thermoplastic, photoplastic and solid-state light valves

Electroluminescent matrices

Opto-magnetic matrices

Laser systems

Injection-electroluminescence matrices

Major emphasis should be placed on display technologies that can provide an all-solid-state flat-panel display using batch-fabrication techniques and compatible with semiconductor integrated circuit voltage, current, and power capabilities. An ideal condition will exist if a technology meeting these conditions is applicable to both console and large-screen displays.

3 BASIC COMPONENTS OF A DISPLAY SYSTEM

The minimum basic display system usually consists of a visual transducer with its associated addressing and selection circuitry and either a character generator or vector generator to translate digital information from the computer into digital or analog positioning information for the display. The possible functions to be performed in a completely generalized display system were presented in diagram form by Mr. S. Sherr at the Fourth National Symposium on Information Display of the Society for Information Display. [1] The functions of this generalized display system are reproduced in Figure C-1. Specific display systems that have been implemented to date do not include all of these functions but most of them are found in one or more systems.

The components of a display system depend upon both its application and its mechanization. [5, 6] For example, a large-screen film based display system might include a symbol generator for converting digital information to a shaped symbol or alphanumeric character, a vector generator for graphical information, an image generator for positioning symbols and vectors properly to form the desired image to be projected on the screen, a photographic system for preparing slides or film from the image generator, a slide or film storage and handling system for moving the appropriate slides to the projector, a projection system for projecting computer generated overlays and map backgrounds, and a screen for viewing the projected display. [7, 8, 9, 10] This is illustrated in Figure C-2. On the other hand, the simple CRT monitor console illustrated in Figure C-3 may include only a raster scan generator, modulation circuits, deflection circuits, and the CRT. In some low cost display systems where several users are working with individual consoles, significant economies have been achieved by providing a separate control and storage module that services several of the individual displays on a multiplexed basis.
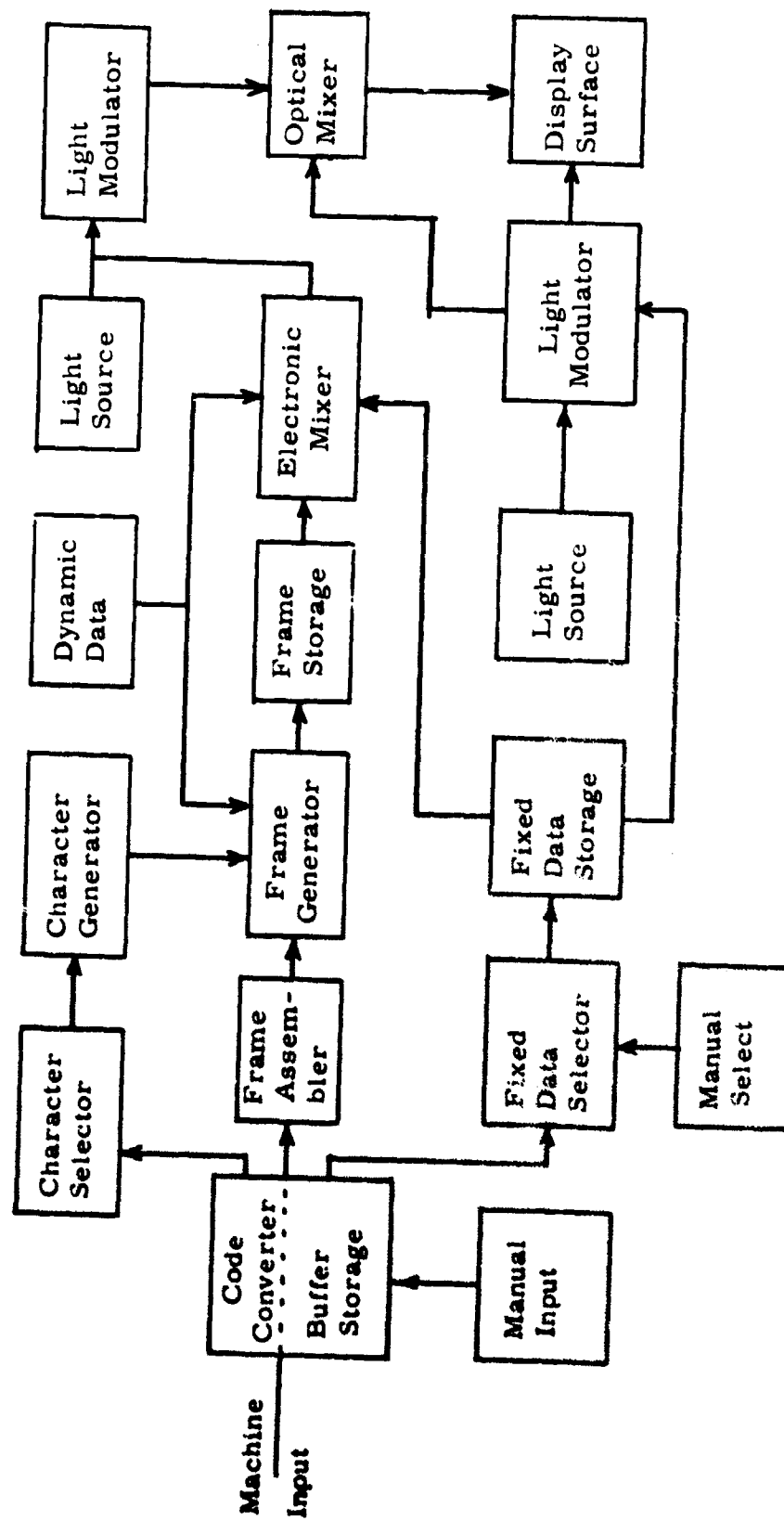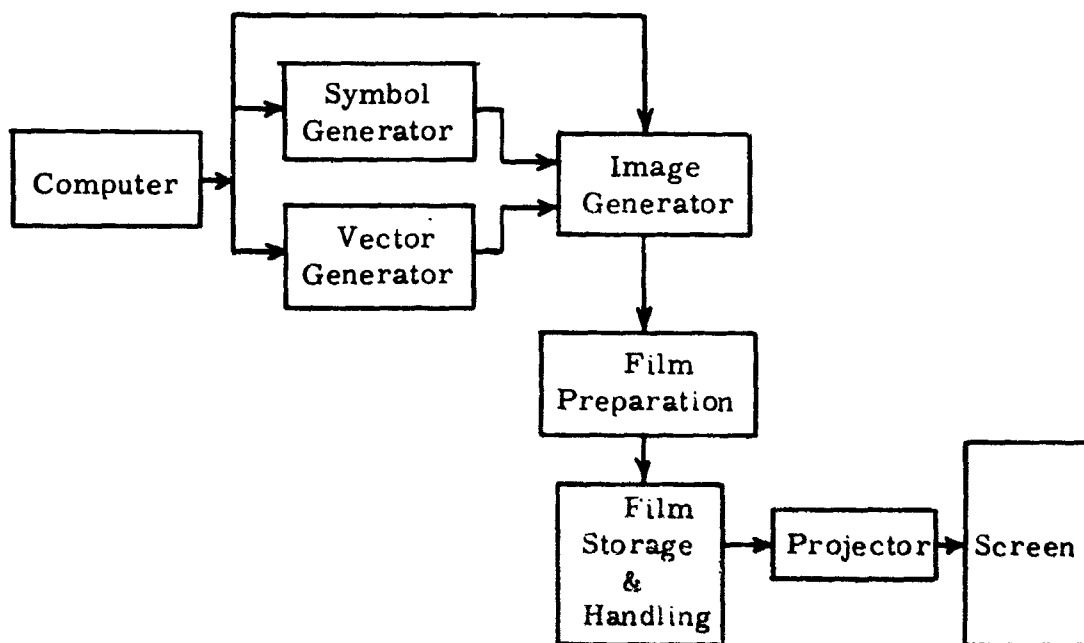
Figure C-1 GENERAL DISPLAY SYSTEM
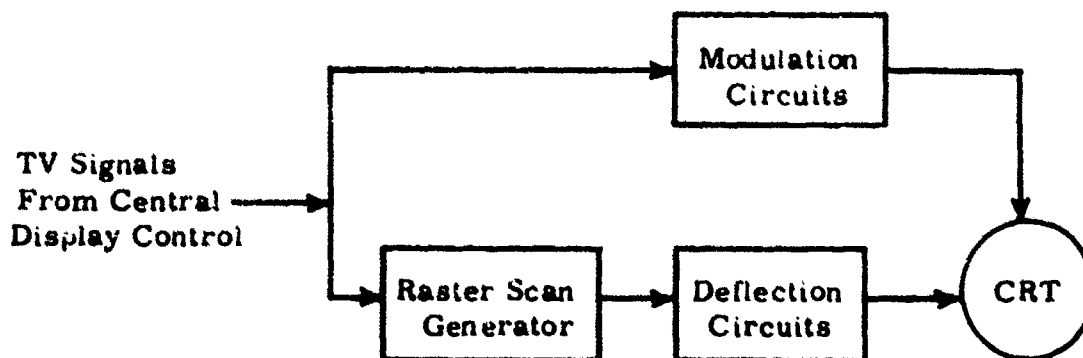
Figure C-2   TYPICAL FILM BASED SYSTEM

Figure C-3   SIMPLE CRT MONITOR

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A complete display console or large-screen display system may also include optional features such as an alphanumeric keyboard, a graphic input device (e.g. , a light pen or a RAND tablet), digital storage, format controls, function switches, and communication facilities for transmitting and receiving information. [11, 12, 13, 14] The display portion of the console usually includes the visual transducer, a character or symbol generator, and selection, addressing, and control logic. It may also include optional features such as a vector generator, a map generator, an overlay generator, and a matrix or coordinate generator. The functions and options included in the display system depend upon the requirements of the application and the cost that can be justified. In addition to the equipment in the display system itself additional storage and processing capability is required in the computer. Although some of the more sophisticated graphical displays are necessarily expensive at present it should be possible to develop techniques for very low cost displays where performance requirements can be relaxed and the logic of the system can be adapted to existing high volume production displays rather than designing special purpose displays to fit into a predetermined system. For example, the modulation, deflection, and CRT portions of a conventional home television receiver are made in large quantities and can be purchased for under $50. 00. However, little effort seems to have been directed toward development of display logic and controls that can utilize this readily available display equipment.

Although not a physical hardware component of the system, programming is a very important aspect of any computer generated display system. [11, 15, 16, 17, 18, 19] The amount of storage space required to store the programs related to the display and the machine time required to process them are frequently underestimated. General programs and subroutines required include:

Executive Control	Storage and Retrieval
Utility	Input/Output
Diagnostic	

Query languages and problem oriented languages are needed that include
user function routines such as:

Rotation	Format Control
Scaling	Format Generation
Translation	Grid Generation
Dimensioning	Pen Location

In a sophisticated large-scale system tens of thousands of works of
storage may be devoted to storing such display programs and routines.

The discussions of display parameters and technologies that follow will
be devoted exclusively to the visual transducer portion of display
systems. However, the reader's attention is directed to references
that provide greater details on other components of a display system
such as character and symbol generators,[20] light pens,[14] the
RAND tablet,[21] and other graphic input devices.[22, 23, 24, 25]

4 DISPLAY PARAMETERS AND CHARACTERISTICS

Characteristics of importance in display systems include:

Response Time	Viewing Area and Configuration
Update Time	Flicker Rate
Symbol Generation Rate	Character and Symbol Repertoire
Line Drawing Rate	Line Drawing Capability
Brightness	Format Capability
Contrast Ratio	Color Capability
Screen Gain	Flexibility
Linearity	Format
Resolution	Capacity
Accuracy	Storage and Regeneration Requirements
Registration	Weight
Stability	Size
Legibility	Power Requirements
Image Quality	Reliability
Screen Size	Environmental Conditions

The photometric and qualitative aspects of visual transducers and their effect on the viewer have been well covered by Stocker and Luxenberg.[26, 27, 28] The relationships between ambient light, brightness, contrast, and legibility are of particular importance in the design of visual transducers. Comparisons of brightness and contrast ratio for different systems are almost meaningless unless they are stated within the context of some assumed or specified ambient lighting conditions. Since it is usually necessary to read hard-copy or printed information in the same room in which one is viewing a display, equal readability for hard-copy and self-luminous displays has been suggested as a criterion for selecting brightness and background illumination.[26] It is important to note that the selection of

display characteristics and parameters and the combination of these in a system is a function of the application and the requirements of the system. For example, lesser brightness can be tolerated and still provide an adequate contrast ratio in a display that is viewed in a semi-darkened room while a much higher brightness is necessary if the application requires that the display be used in daylight.

Typical characteristics desired for high performance large-screen displays are:

Size	6 x 8 ft.
Brightness	20 to 25 ft. -lamberts
Viewing Angle	$\pm 40^{\circ}$ at half brightness
	$\pm 60^{\circ}$ at one-third brightness
Color	2 or 3 colors desirable, but may be sacrificed for size, cost, and maintainability
Linearity	0. 2 to 0. 5%
Rapid Update (Blink Time)	$\angle 1$ sec.
Resolution (Optical)	2, 400 optical lines (if photos or maps required)
Resolution (Digital)	512 to 2, 048 positions in X and Y
Symbol Types	64 to 128 plus vector drawing capability
Symbols Generation Speed	20, 000 to 100, 000 symbols/sec.
Contrast Ratio	50 : 1

The following comments amplify and explain some of the characteristics listed in the preceding tables:

<u>Brightness</u>   20 to 25 foot-lamberts approximates the brightness of a sheet of newsprint on a properly illuminated deck.

Viewing Angle A viewing angle of 80° is the best that can be obtained (for half brightness) with a rear projection screen with a gain of one. Lower gain screens are undesirable because the combination of lower gain and higher reflectivity degrades the contrast.

Color Three colors plus white are desirable but two may suffice. The number of colors, and even the use of multi-colors, may be sacrificed to minimize the amount of equipment and hardware desired.

Resolution (Optical) 1200 TV lines will permit 80 lines of characters (at 15 lines/character). Since 600 optical lines correspond to 122 TV lines, the 2,400 optical lines are more than enough for 80 lines of characters. However, if photos or maps are required on the same display, 2,400 optical lines are marginal. Screen width of 8 feet is approximately 100 inches; hence, there are 25 lines per inch on the screen. The eye can resolve 250 lines per inch at 10" distance; hence, at 100 inches (or 8 feet) lack of resolution will be apparent - i. e., 8 feet is the nearest viewing distance. To get 2,400 optical lines on a film with 60 1/mm resolution (typical of color film) requires a 40mm format. It can be done easily on a 70 mm film chip.

Symbol Generation Speed 80 lines of 100 characters requires 8000 characters per second. If the display must be refreshed at 48 cycles/ second for a flicker threshhold of 20 foot-lamberts, the characters per display must be multiplied by 48 to get the character rate. This gives 384,000 characters per second. Hence, a display that must be regenerated at flicker-free rates would require a higher symbol generation speed or would permit displaying fewer characters. The rates shown are sufficient for a display with inherent storage or for a regenerated display with graphical type drawings and fewer characters.

Contrast Ratio   5,000 lumens will produce 100 foot candles on a 50 square foot screen (6' x 8'). With a screen gain of one, the initial brightness is 100 foot-lamberts. Using a 4x neutral density filter coating over the screen will cut this to the 25 foot-lamberts shown. The 4x filter, traversed twice, and the 50% reflectivity factor of the screen will produce a 32x attenuation of ambient light. Thus 16 foot candles of ambient light are permissible since the ratio of 25 foot-lamberts to 1/2 foot-lambert (reflected ambient) gives the 50:1 contrast ratio.

Typical characteristics desired for high performance, on-line, alpha-numeric and graphic display consoles are:

Display Surface	15 x 13 to 20 x 17 inches
Character Size	0.1 to 0.5 inches
Symbol Types	64 to 256 plus vector drawing capability
Symbol Generation Rate	50,000 to 500,000 symbols/sec.
Line Drawing Rate	500,000 to 1,000,000 inches/sec.
Refresh Rate	50 to 60 frames/sec.
Random Positioning Time	3 to 15 usec.
Resolution (Digital)	512 to 2,048 lines
Spot Size	10 to 20 mils
Position Accuracy	0.5 to 1%
Linearity	0.5 to 1%
Brightness	40 to 60 ft.-lamberts
Contrast Ratio	20 : 1 to 40 : 1

Typical characteristics desired in a low cost remote display are:

Display Surface	6 x 4 to 12 x 9 inches
Character Size	0. 07 to 0. 2 inches
Symbol Types	64 to 128
Symbol Generation Rate	15,000 to 30,000 symbols/sec.
Line Drawing Rate (optional)	20,000 to 100,000 inches/sec.
Refresh Rate	30 to 40 frames/sec.
Random Positioning Time (optional)	20 to 40 usec
Resolution (Digital)	256 to 1,024 lines
Brightness	25 to 50 ft. -lamberts
Contrast Ratio	20 : 1 to 30 : 1
Display Screen Capacity	500 to 2,000 characters

Both large screen displays and console displays for naval tactical systems
should also have reliabilities in the order of 2,000 to 10,000 hours
MTBS and be capable of meeting MIL-E-16400. These are very severe
requirements for the large-screen display techniques in use today, but
several solid-state display technologies offer promise for meeting these
requirements in the 1970 to 1980 time frame. Xenon lamps used in
film-based systems have MTBF of 2,000 hours. Replacement time is
10-15 minutes. It is hoped that some of the new technologies will
provide higher reliabilities and better maintainability (MTBF's in excess
of 2,000 hours and MTR's less than 10 minutes), but these are minimum
goals.

It is questionable whether low-performance, low-cost remote displays
will be required in future naval tactical systems, but if they are, storage
tubes may be attractive in lieu of a digital buffer. Although a storage tube
is more expensive than a conventional CRT, the use of one would significantly
reduce the necessary character generation and line drawing rates in remote
displays by eliminating the need for recreating the image 30 times per second
to refresh the screen.

5 DISPLAY TECHNOLOGIES

Although many different approaches have been taken to implementing visual transducers, cathode ray tubes are by far the dominant technology. Most of the research and development work on display technology is pointed toward large-screen displays because of the inadequacy of present techniques. However, there is also interest in improved technologies for console displays that will permit a flat panel display (visual transducer) that is compatible with integrated circuits and other batch-fabrication technologies for addressing, selection, and control. It is impractical to consider here all of the approaches that have been investigated for implementing visual transducers, but some of the more important or more promising display technologies presently in use or in the research and development stage are compared in Table C-1. Others are discussed in several previous summaries or surveys of display technology.[29, 30, 31, 32, 33]

The difficulty of establishing quantitative measures of display system effectiveness is one of the major problems in the display field which makes comparison of widely different technologies very difficult.[6] The values shown in Table C-1 for brightness and update time are typical of those that can be achieved, but for some of the technologies these characteristics may vary widely above and below these values. The columns referring to the use as large-screen or console displays is a relative one. For example, since the CRT is so satisfactory as a console display many of the other technologies are not relatively well suited to console displays; on the other hand, since none of the large-screen techniques are entirely satisfactory several of them can be considered good on a relative basis. These two columns do not refer to performance but merely to their suitability for large-screen or console images. For example, mechanical inscribing systems and film projection systems are good ways to generate large-screen images, but

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Display Technology	Relative Use As A		Brightness (Ft-lamberts)	Update Time	Color Capability	Feasibility	Reliability and Life
	Large Screen	Console					
Cathode-Ray Tube	Poor	Best	40	1/30	Color tube can be used	Readily available	Good
Mechanical Inscribing Systems	Yes	No	25	1 to 2	Filters and multiple projectors	Readily available	Poor
Film Projection Systems	Yes	Possible	25	5 to 15	Filters and multiple projectors; lenticular film	Readily available	Poor
Photochromic-CRT Display	Good	Good	20	<1	Filters or different color photochromes	In prototype stage	Good
Oil-Film Light Valves	Yes	No	20	1/30	Filters and multiple systems	Available	Poor
Thermoplastic and Photoplastic Light Valves	Good	No	20	1/30	Filters and multiple systems	In prototype stage	Good

SUMMARY OF CHARACTERISTICS OF DISPLAY TECHNOLOGIES

TABLE C-1

| Display Technology | Relative Use As A | | Brightness (Ft-lamberts) | Update Time | Color Capability | Feasibility | Reliability and Life |
	Lg. Screen	Console					
Solid-State Light Valves	Good	No	Not available	Not available	Filters and multiple systems	Uncertain	Unknown
Electroluminescent Matrices	Good	Good	20	1/30	Multiple-dot color using different color phosphors	By 1970	Fair
Opto-Magnetic Matrices	Good	Good	50	<1	Color is a function of reflection angle	By 1970	Good
Laser Inscribing Systems	Good	No	25	<1	Filters and multiple projectors	By 1970	Good
Laser-Luminescent Displays	Good	Possible	Not available	Not available	Unknown	Promising	Unknown
Injection Electro-luminescence Matrices	Good	Good	Not available	Not available	Unknown	Promising	Unknown

SUMMARY OF CHARACTERISTICS OF DISPLAY TECHNOLOGIES

TABLE C-1

(Continued)

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they are both slow and have other disadvantages compared to some of the other technologies shown.

In considering the comparisons shown in Table C-1, it is important to remember that the selection of an appropriate display technology is not made on the basis of one or two characteristics but rather on the composite ability of the technology to best meet the needs and requirements of the specific application. Navy systems planners should give greater or lesser weight to individual parameters depending upon the requirements of the specific application. They may also need to consider additional factors that are peculiar to his application.

It is necessary to make compromises in some characteristics in order to accept a display technology that meets other essential requirements more important to the particular application. A decision as to whether to use a multi-color system in a large-screen display is an example of the compromises that must be made. The use of several colors in a display offers definite advantages in terms of the ability to distinguish different types of items (e. g. , in a simple case, friendly and hostile forces); hence, from the user standpoint a multi-color system is desirable. However, a color display usually involves a significantly greater amount of equipment and hardware which implies an increase in space and cost (and probably adverse effects on reliability and maintainability). Hence, the Navy systems planners must balance the need for multi-color displays from the user standpoint against the penalties that may result in other performance characteristics, in cost and size, and in reliability.

On the basis of the comparisons in Table C-1, the most promising technologies for mechanizing the visual transducer portion of display systems in the future include:

Cathode-ray tubes

Photochromic-CRT displays

Thermoplastic, photoplastic, and solid-state light valves

Electroluminescent displays

Opto-magnetic displays

Laser systems

Injection electroluminescence matrices

Mechanical inscribing and film projection systems are the major large screen display technologies available today.[30] However, these approaches to large screen design suffer from problems of size, cost, reliability, maintainability, and cost of the expendable media. Hence, although these are the only practical techniques available today on a production basis, they will be replaced by newer technologies, such as those listed above, within the next few years. These newer technologies are discussed in greater detail later.

Developments presently underway in integrated circuits and batch-fabricated memories are creating a revolution in computer technology; hence, effective low cost displays will be required if displays are to fulfill their promise of providing close man-machine interaction without limiting size, weight, cost, and reliability improvements in future naval tactical systems. Since integrated circuits and other batch-fabrication technologies will be used to implement the digital logic, storage, and control functions in displays, a premium will be placed on visual transducer technologies that are compatible with them. These batch-fabricated electronic and magnetic technologies are most

effective in implementing low voltage, low power, and low precision components. They are poorly suited to the requirements of most of the approaches to the implementation of visual transducers in use today. Table C-2 provides an indication of the compatibility of several visual transducer technologies with batch-fabricated computers anticipated in the near future.

Predominantly electromechanical technologies, such as film projection systems and mechanical inscribers, are particularly vulnerable to obsolescence in this respect. Those involving bulky electronic and optical equipments such as cathode-ray-tubes, photochromic-CRT systems, and projection light-valves are also vulnerable. From this standpoint of compatibility with solid-state electronic and magnetic component technologies, crossed-grid electroluminescent panels with integrated storage, matrix controlled opto-magnetic panels, and injection electroluminescence matrices appear most promising.

5.1 Cathode-Ray Tubes

Cathode-ray-tube technology was well advanced before the advent of computer generated displays as a result of many years prior experience in applications such as radar, oscilloscopes, and commercial television. Not only are CRT's the dominant technology for console displays, but they also play an important role as the image generator in a number of large-screen display technologies. For example, in a film-based projection system for large-screen displays the image is initially generated on a small high precision CRT prior to its transfer to film by a photographic process. Another example is the photochromic-CRT system discussed later in which the image is again initially formed on a CRT to modulate the photochromic media which serves essentially as a light valve.

	Low Voltage	Low Power	Small Volume	Digital Selection	Low Cost	Adaptability to Batch-Fabrication
Cathode-Ray Tube	Poor	Poor	Poor	No	Fair	Poor
Electro-luminescent	Poor	Fair	Good	Yes	Good	Good
Opto-Magnetic	Good	Good	Good	Yes	Good	Good
Laser-Luminescent	Fair	Fair	Fair	Yes	Fair	Poor
Injection Electro-luminescence Matrix	Good	Good	Good	Yes	Good	Good

ANTICIPATED COMPATIBILITY OF VISUAL TRANSDUCER TECHNOLOGIES

WITH BATCH-FABRICATED COMPUTERS

TABLE C-2

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The numerous CRT-type devices that have been developed provide great flexibility and versatility in the use of CRT's in display systems.[30, 34] The Charactron tube provides character and symbol generation by selectively positioning the beam to shine through the appropriate symbol on a character mask prior to positioning on the face of the tube without the need for external electronic character or symbol generators.[35] Storage tubes provide the ability to store an image on the face of the tube without separate digital storage.[36, 37, 38] Scan conversion tubes permit the conversion of an image generated in one format (e.g., by means of a Charactron, an analog vector line drawing system, etc.) into a TV type raster scan format.[39, 40] Another special purpose tube provides a clear port in the rear of the tube through which a photographic image can be projected onto the inside of the face plate to permit imposing a computer generated electronic image on a photographic image such as a map background.[41] A number of other special types of CRT's offer advantages in certain types of display functions. Advantages accrue to display system designers from both the prior effort that has been expended in the development of CRT's and also from the prior effort and large body of existing knowledge about the associated electronic circuits and optical properties.

Although they represent the most satisfactory display technology for console displays, CRT's suffer from at least six disadvantages in display system applications:

1. For practical purposes the screen size is limited to 20 to 30 inches

2. The physical volume of the tube is large because of its three dimensional nature, the envelope, and the need for a relatively long tube to provide high quality electron optics.

3. The requirements for high voltage and high power for selection and modulation circuits are not compatible with integrated circuit semiconductor technology.

4. The ultimate resolution and registration is limited by the basic analog nature of the deflection electrodes and their associated drivers. At best, addressing can only be pseudo-digital.

5. The device is not inherently suited to high shock and high vibration environments for military applications although significant progress has been made in handling these problems by relatively brute force techniques.

6. A refresh rate of at least 30 frames per second is necessary to avoid noticeable visual flicker. Even with long persistence phosphors flicker is noticeable at rates less than 30 frames per second. There is no inherent long term storage in CRT's, except for relatively expensive special storage tubes.

Some of the problems cited above make direct view CRT's inherently unsuited for large-screen displays. The other problems will eventually lead to the replacement of CRT's, even in console displays, by some flat panel display technology where the elements of the screen can be batch-fabricated and provide inherent digital addressing and selection matrices. Examples of such technologies are crossed-grid electroluminescent matrices, magneto-optic panels, and injection electroluminescence diode matrices. In the long run some flat panel display technology that can also provide an inherent storage capability will probably become dominant for both console and large-screen displays.

5.2 Photochromic-CRT Displays

Photochromic films have three properties that permit them to be used in real-time dynamic or plotting type displays where silver-halide and Kalvar films cannot be used easily. These properties are:

1. A reversible process, hence eraseable and reuseable
2. Self-developing, hence requires no processing
3. Relatively insensitive to ambient light, hence can be exposed without light shielding (if the ambient light does not contain significant amounts of ultraviolet or infrared)

Most photochromic materials are organic dyes that become opaque when exposed to ultraviolet light, and return to the transparent state when exposed to heat or infrared light. By coating a transparent film (e.g. mylar) with a thin layer of photochromic material, a "photographic" type media can be produced in which the chemical process is reversible. Recently an inorganic photochromic glass has been developed that is more promising for display applications since it does not fatigue as the organic dyes do.[42, 43] An image can be exposed with ultraviolet light and erased with infrared light in most photochromic materials.

At room temperature, the exposed image will decay at rates depending on the particular chemical compound. Typical persistence times for photochromic materials used in display systems range from a fraction of a second to 15 minutes. The faster decay times require regeneration of the image. Longer persistence times can be achieved by cooling the image since the decay is inhibited by cold temperatures and enhanced by heat.

Combining a cathode-ray-tube with the photochromic film permits the electronic generation of an image. A fiber-optic face plate CRT can

be used to generate an image on the outer surface of the face of the tube by conventional techniques.[44, 45] A dichroic mirror is sandwiched between the fiber-optic face plate and the photochromic film. The ultraviolet light from the phosphor on the inner surface of the face of the CRT is transmitted through the fiber-optic face plate to generate an opaque image on the photochromic film. Visual light from an external source is projected through the photochromic film onto the dichroic mirror which reflects it back through the photochromic film onto a viewing screen. The opaque image on the photochromic film prevents the light from the projector from striking the dichroic mirror. Hence, this image is reflected onto the screen. Since the light passes through the photochromic film twice, the optical density is effectively doubled.

For dynamic applications such as target tracking, this technique not only permits a real-time target track, but also provides target track history in the form of a trace with "intensity" decreasing with time. The time period covered by the visible target track history is a function of the photochromic material. At the present time, the speed of photochromic materials limits the character generation rate to less than 100 characters per second.

Successful development of faster photochromic materials will provide an attractive electro-optical dynamic large-screen display with no mechanically moving parts. This approach to photochromic displays also offers promise for improved console displays by permitting a very small diameter, high resolution CRT to be used as the image source with the image projected onto the rear of a console size screen.

5.3 Light-Valve Systems

The term "light valve" in a generic sense refers to any system in which light passing through the system is modulated. The photochromic-CRT system is a light valve in that sense. However, the term is usually used in a narrower sense to refer to a cathode-ray-tube projection display system using a Schlieren optical system or to certain types of liquid or solid crystal devices.

The most common example is the "oil-film" light valve used in theatre projection TV systems. The problem of cathode contamination caused by the presence of an oil film in the vacuum chamber of such systems can be avoided by the use of thermoplastic and photoplastic media in light-valve systems.

An electron beam in an evacuated cathode-ray-tube type device can be used to write on a thermoplastic media by depositing electrons on the surface. If the film has been heated to the softening point, the electrostatic forces cause the surface of the film to become distorted in a pattern corresponding to the image. This image is projected with a Schlieren optical system, as in the case of an oil-film light valve. A television type raster scan is normally used. Special cathode-ray-tubes with wire face plates have also been used in such systems so that the electrical charge can be brought outside the cathode-ray-tube to eliminate the need for placing thermoplastic media in the tube.[30] Another type of thermoplastic light valve uses an XY matrix of electrodes rather than a cathode-ray-tube to record on the thermoplastic media.[46] In this type of "in-air" thermoplastic system, signals on the X and Y matrix wires deform the thermoplastic and a TIRP (total internal reflection prism) projection is used to project the image from the thermoplastic material on to a large screen.

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Photoplastic media combine photoconductive and thermoplastic techniques.[47] A conducting layer, a photoconductive layer, and a thermoplastic layer are used. If the thermoplastic layer is transparent and the media is exposed to a light pattern in the form of an image, the charge from the conducting layer can move through the photoconductor in the areas corresponding to the light pattern. If the surface of the thermoplastic layer is first charged with respect to the conducting layer prior to the exposure to the light image and then discharged to the conducting layer after exposure, a charge pattern is retained on the surface of the thermoplastic film. This charge pattern on the thermoplastic film corresponds to the light image as a result of the charge pattern in the photoconductive layer. Heating the plastic permits the electrostatic forces to deform the thermoplastic surface.

A Schlieren optical system may be used to project this image also, but the photoplastic media offers an important advantage cver the straight thermoplastic media. Since the recording is by light rather than by electron beam, it is not necessary to place the photoplastic media inside the vacuum chamber. This permits an "open-air" light-valve system that avoids many of the disadvantages of oil-film and some thermoplastic light valves which require that the media be within the evacuated envelope.

Using the light from the face of a cathode-ray-tube to write on a photoplastic media. when combined with a Schlieren optical system for projection, provides a dynamic, real-time, large-screen display with a sealed vacuum system and reuseable media. Heat is utilized for both instantaneous development and for erasure. Resolutions of 360 line pairs per millimeter, spot size of approximately one millimeter, and contrast ratios in the order of 30:1 have been achieved with photoplastic light valves.

Solid-state light valves are an interesting and promising technique for long-range consideration since many of the problems associated with oil-film, thermoplastic, and even photoplastic light valves, do not occur. In some approaches, even the necessity for a cathode-ray tube may be avoided.

One approach that has been proposed uses a solid-state crystal for light modulation but it is not really an all-solid-state device since a cathode-ray tube is used to control the crystal.[48] In this approach, the electron beam controls the passage of light through a birefringent KDP crystal in the face of the tube. A polarized light is projected through a rear window in the CRT, through the crystal modulating element in the face of the tube, through an analyzer, and onto a screen. The polarizer is oriented at 45° and the analyzer at minus 45° with respect to the sides of the crystal. The polarization vector of the plane polarized light incident on the crystal is rotated when the crystal is biased by the electron beam. The electron gun in the CRT generates an image on the crystal modulator: the polarized light passing through the modulator then projects this image onto the screen. The electron gun serves as a control element but is not required to supply the light output. Resolution of 250 TV lines per inch, contrast ratios in excess of 150:1 and optical efficiency of 5% have been reported from laboratory models.[49]

A crystal light modulator is one example of a class of light modulators where electrical or magnetic fields are used to modify the optical properties of an electro-optically active crystal (or liquid in some approaches) - properties such as transparency, index of refraction, plane of polarization, color, etc. Although the media controlling the light is solid-state, the media itself must be controlled by some

method to generate the image. The most practical method of accomplishing this at present is with a cathode-ray tube. In the more distant future, a low-power laser may be used to control the crystal, which in turn controls the light from a high power optical projection system.

5.4 Electroluminescent Displays

Electroluminescent displays offer the advantages of an all-solid-state display without moving parts or projection optics, a flat display requiring very little depth, and sufficient brightness for viewing under properly controlled room lighting conditions.

Aside from discrete character displays, the electroluminescent display which has been developed further than others to date is the electroluminescent crossed-grid display.[50, 51, 52] This display uses a continuous electroluminescent sheet with the electrodes on one surface subdivided into parallel strips in the X direction and the electrodes on the other surface subdivided into parallel strips in the Y direction. Applying excitation to an X and a Y strip will cause the electroluminescent material to emit light at the intersection, and to a lesser degree, along each strip. The contrast ratio between the light output at the intersection and that along each line is approximately ten to one. To reduce this "cross-effect," a continuous sheet of non-linear resistor material is coated on the electroluminescent material between the two sets of electrodes.[53] This increases the contrast ratio between the light output at the intersection and that along each line and reduces the capacitance and hence the driving power required.

This approach is useful for both large-screen and console type displays. Real-time dynamic displays, such as target tracks, can

be generated by properly sequencing the selection of X and Y grids. Alphanumeric characters and symbols can be drawn on the same display. However, it is necessary to regenerate each spot on the display periodically since it has no storage characteristic. As a result, this type of display requires either an external storage or computer controlled regeneration. To avoid noticeable flicker, the picture must be regenerated in excess of 30 times per second. This creates a serious problem in switching and distributing the signals in a large display panel. [54] The frame rate and the time required to energize each spot on the display limit the total number of positions that can be activated. Activating too many positions may decrease the level of light output if each spot is not energized for a long enough period and sufficiently frequently. Periodic action is required for active spots that remain static as well as for those that are changing. A typical mosaic panel with pulses of 20 usec duration and a frame rate of 30 per second provides an average 20 foot-lamberts of luminance. Resolutions of 50 to 100 lines per inch are considered feasible.

To overcome the necessity for regenerating the entire display periodically, considerable attention has been given to the development of matrix addressed electroluminescent display panels that include a storage capability for each position on the display rather than an external storage such as a core matrix. A method is required that provides individual storage directly coupled to each position so that individual positions can be turned on and will remain on until intentionally turned off. Two different approaches have been taken to this problem. The first is to fabricate a display panel with a matrix of discrete electroluminescent elements, each having an associated semiconductor storage circuit. An XY selection matrix is used to turn on the storage element which energizes a

specific electroluminescent element and holds it in that state until
it is cut off by another XY selection operation. Resolution of 16 to
20 lines per inch are considered feasible. This approach provides
a true dynamic large-screen display with exact registration and
positioning, without mechanically moving parts, and without an
optical projection system. However, it is quite expensive due to
the electronic selection of individual elements and the electronic
storage associated with each element. Development of an integrated
circuit storage array may lower the cost of the electronic elements,
but it would still be necessary to make physical connections between
each bit of storage on the semiconductor chip and the corresponding
electroluminescent element.

The major fabrication and cost problems associated with this type of
electroluminescent storage panel result from the use of an individual
semiconductor storage circuit for each spot on the display. A
different approach alleviates these problems by overlaying a sheet
of electroluminescent material with another sheet of material that
provides storage in conjunction with the electroluminescent material.
Electroluminescent elements and photoconductive elements have been
combined for this purpose. The electroluminescent element provides
sufficient light to keep the photoconductive element in the conducting
state, while the photoconductive element provides a path for keeping
the electroluminescent element energized. The result is an EL-PC
storage element with both electrical and optical feedback. The
ability to fabricate the storage media directly on the electroluminescent
panel without the necessity for making connections between each
display position and its storage element offers promise for a more
desirable solution. Approximately 20 lines per inch resolution is
anticipated in future devices.[50]

5.5 Opto-Magnetic Displays

A different approach to solid-state displays is based on the magnetic properties of certain thin-film materials (e.g., RIS 1 films) which cause "stripe" domains that can be turned on or off by the application or removal of a magnetic field. [55, 56] If a colloidal suspension of proper material (e.g., magnetite) is put over the thin magnetic film, the magnetic stripe domains align the Bitter particles of the colloidal suspension which then form an optical diffraction grating. Using an XY selection matrix defines individual display elements at each intersection of the X and Y wires. The display elements are switched on and off by coincident current selection in the XY matrix as in a thin magnetic film matrix memory. [57, 58] When the display panel is lighted from the side by a high intensity line source, the elements that are switched on magnetically reflect light brightly while those that are switched off remain dark. The XY selection matrix is used to form symbols and vectors by proper choice of the individual display elements that are switched on to form the image.

A line source of light is normally used to prevent the angle of viewing from being critical. However, since the color of the reflected light is a function of the viewing angle with respect to the screen and the light source, color displays can be achieved by taking advantage of the diffraction effect.

Element switching speeds of less than 10 microseconds, brightnesses of over 100 foot lamberts, contrast ratios of 70:1, and resolutions of 100 elements per inch are anticipated. Opto-magnetic displays of this type provide a digitally addressed flat panel display with inherent storage in the magnetic film. Since the light is reflected by the display element rather than being switched by the electronic components, this type of

display is quite compatible with batch-fabricated electronic and magnetic components, and the display panel itself is adaptable to batch-fabrication techniques.

5.6 Laser Systems

Lasers offer great promise for future implementation of display systems - particularly large-screen displays. The ability of a laser to deliver highly concentrated light energy in a coherent beam of very small spot size is well known.[59, 60] Several different approaches to laser displays are being investigated.[61] Since they all require some means for deflecting and modulating the laser beam, considerable development efforts are being expended on deflection techniques.[62, 63, 64, 65, 66] Digital deflection of lasers by crystals has been satisfactorily demonstrated for 256 positions in each direction, but at least 1024 positions in each direction are needed for a practical large-screen display system.

Laser inscribing systems are being developed that are similar in concept to a mechanical inscribing system. In place of a mechanical stylus, a laser beam is used to inscribe by vaporizing a metallic film on a glass plate. The vaporization of the metal on the glass plate by the laser beam permits light to shine through, projecting the image on the screen. This approach may provide the first use of lasers in large-screen display systems since it requires neither the intensity needed in a direct viewing laser-luminescence system nor the generation of an ultraviolet laser beam needed for a photo-chromic system.

A combination photochromic-laser display has been proposed that may be feasible soon. In this approach, an ultraviolet laser beam is

digitally deflected to write on the photochromic material. This combination can provide a very high resolution since a 10 to 20 micron spot size can be obtained with a laser beam compared to a 1 mil spot size for a cathode-ray tube.

Another attractive approach is the use of a laser beam to write directly on a large luminescent screen. This is somewhat equivalent to an "outdoor" cathode-ray tube in which the laser beam replaces the electron beam and the luminescent screen replaces the phosphor face plate of the tube. It offers advantages over a CRT in that a vacuum is not required and a large-screen image can be generated directly. One feasibility system has been developed using a 50 milliwatt neon-helium gas laser. a KDP crystal modulator, a piezoelectric crystal driven horizontal deflecting mirror, and a glavonometer driven vertical deflecting mirror to provide a TV rastor scan image projected onto a 40 inch screen.[67] Brightness of 50 foot lamberts. contrast ratio of 100:1 (dark environment), resolution of 1,000 to 2,000 lines, and update time of 33 milliseconds are anticipated for direct view laser systems.

A display screen with controlled persistency described by Graff and Martel appears very attractive for use with an ultraviolet laser in a system similar to that described above.[68] An active screen reduces the laser power required. The ability to control the persistence of the image on an electroluminescent panel offers some interesting possibilities for some applications. For example, when viewing a display showing only the immediate real-time image, historical data (such as target track history) could be recaptured by changing a switch setting.

Two major development problems associated with laser displays are:

.   Obtaining sufficient power at the desired wave length
    to provide adequate luminance at the desired color, and

,   Obtaining deflection and intensity modulation devices with
    sufficiently fast response to provide the necessary resolution.

Hence, the power and efficiency available from lasers at the desired wave lengths (particularly ultraviolet) must be improved, and adequate laser deflection techniques must be developed before laser displays will be feasible for widespread use.

5.7 Injection Electroluminescence Matrices

Very little information has been published on injection electroluminescence matrix displays, but from a long range standpoint they offer a very promising method for implementing both large-screen and console displays.[69, 70, 71] Such a system uses light emitting diodes in a matrix arrangement to form a solid-state display panel that can provide high resolution and that is compatible with batch-fabricated electronic and magnetic components. It is likely that the display panel can also be batch fabricated. The panel would consist of an array of electroluminescence diodes (e. g. , gallium-arsenide-phosphide) controlled by integrated circuit arrays. The successful development and production of this type display panel is farther away than others discussed here, but this technology should be followed closely for applications in future naval tactical systems.

5.8 Three-Dimensional Displays

For some applications 3-D displays are desirable, but no really satisfactory 3-D displays have been developed. Several approaches have been proposed and some models have been built.[72, 73, 74] Holograms offer an interesting possibility for future 3-D displays but practical applications are at least several years away.[75, 76, 77]

6 PROBLEM AREAS AND FUTURE PROGRESS

Closer-man-machine interaction will permit the computer to act as
an amplifier of human intelligence rather than merely as a sophisticated
calculator and record keeper. Achieving this interaction will require
the ability for the human to ask questions and give instructions to the
computer in both graphical and alphanumeric form; to receive formatted
data, graphs, and suggested courses of action from the computer; and
to make decisions and change his course of action repetitively with
appropriate feedback from the computer on a real-time basis. This
close man-machine interaction will require effective, low cost, high-
speed displays. Unfortunately, display (i.e., visual transducer)
technology, as well as that in other input-output areas, has not kept
pace with advances in digital electronic and magnetic technologies.

Although the display field has progressed rapidly during the past five
years, significant future progress is still required to provide the type
of displays necessary to achieve the close man-machine interaction
that will be essential in future naval tactical systems at a price that
will permit their widespread use. Several major needs and problems
facing the display field have been discussed here which include the
need for:

> Better methods of implementing large-screen displays that
> can provide dynamic real-time operation with both alphanumeric
> and graphical data.

> Flat panel visual transducers for both large-screen and
> console displays that:
>> can be addressed digitally
>> provide storage inherent to the display panel
>> are compatible with batch-fabricated electronics and
>> magnetics.

Better determination of the proper functions to mechanize
in the display to facilitate the human interface including the
appropriate human factors determination of the appropriate
trade-offs between manual and automatic functions.

More effective software to both facilitate the programming of
display functions and to provide for the efficient computer
generation and control of operations such as dynamically
using real-time tactical data and interrogating large data
bases.

Lower cost for all categories of displays but particularly
for low performance remote display consoles if these are
required in future naval tactical systems.

Developments or improvements needed in specific display technologies
(e. g., the need for higher power or ultra-violet lasers) have also been
cited.

As these problems are solved, displays will have an increasing impact
on computer utilization. The problems of software, human factors, and
utilization will be solved as additional experience is gained and as
research and development application efforts are expanded. Several of
the advanced display technologies discussed here offer promise of solving
most of the hardware problems. Photochromic, light-valve, laser,
crossed-grid electroluminescent, opto-magnetic, and injection electro-
luminescence matrix displays offer promise for providing real-time
dynamic large-screen displays. The last three are flat panels adaptable
to batch fabrication, and compatible with batch-fabricated electronic and
magnetic components. Opto-magnetic displays have inherent storage while

storage components may be fabricated directly on electroluminescent and injection electroluminescence matrices.

Cathode-ray-tubes will be dominant for console displays for the foreseeable future, but they will ultimately be replaced by one of these techniques or possibly a new technology yet to be developed.

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Appendix D

INPUT/OUTPUT TECHNOLOGY

1 GENERAL

There are three major approaches to improving the performance of future systems with respect to input/output capability. These are:

Improvements in the performance of present types of input/output equipment.

Development of new types of input/output equipment that are not in widespread use at present.

Approaches to system organization that minimize the need for conventional input/output equipment.

Each of these approaches will play a part in performance improvements in future systems. However, unless much greater effort is placed upon the development of non-mechanical input/output equipment, the best hope for future systems lies in developing system techniques that minimize the need for input/output equipment.

This Appendix discusses technical developments affecting each of the three approaches to improving input/output performance outlined above. Emphasis has been placed on new input/output equipment techniques that offer promise for performance improvements in future systems. These investigations have included new devices and techniques (both in the research stage and currently under development) to allow direct entry of data. Also included are the investigation and follow-up of particularly interesting techniques and approaches that were examined briefly in the initial ANTACCS study but that were not pursued in depth due to lack of adequate time to cover all research and development projects of interest. Improvements in conventional types of input/output equipment have also been investigated.

2 IMPROVEMENTS IN THE PERFORMANCE OF PRESENT TYPES OF INPUT/OUTPUT EQUIPMENT

Almost all present types of input/output equipment are dependent on electromechanical action. The requirements of present input/output equipment for this type of action imposes limitations on the improvement that can be achieved through the application of batch-fabrication techniques in electronics and magnetics. Although these electromechanical input/output equipments will limit systems performance, the effect on systems cost and reliability is even more serious. The performance limitations could be overcome to some extent by using a larger number of input/output units, but this further accentuates the cost and reliability imbalance that exists with respect to the central processor and memory.

Performance characteristics anticipated by 1970 for some of the major types of conventional input/output equipment are shown in Table D-1. Examination of these characteristics will indicate performance improvements of less than one order of magnitude and in most cases of less than two-to-one over equipment commercially available today. Punched paper tape is not included in Table D-1 because it is believed that incremental magnetic tape readers and recorders will replace punched paper tape equipment for most high performance applications. Incremental magnetic tape equipment will be cheaper for high performance, will be more reliable, and will utilize tape records and formats that are completely compatible with high speed conventional magnetic tape units. Although block oriented magnetic tape units have been in use since the early days of the computer industry, the ability to economically read and record incrementally opens new applications for magnetic tape input/output. Incremental magnetic tape recorders and readers and their advantages as replacements for punched paper tape equipment are discussed in detail in this sub-section.

Magnetic tape units	300,000-400,000 char/sec read write rate	2000-3000 char/inch density
Incremental magnetic tape		
Recorders	800-1000 char/sec record rate	800 char/inch density NRZI
Readers	500-600 char/sec read rate	800 char/inch density NRZI
Punched cards		
Punches	500-700 cards/min punch rate	
Readers	2000-3000 cards/min read rate	
Line printers		
Impact type (multiple copy)	2000-2500 lines/min	*64 character type font
Non-impact type (single copy)	5000-7000 lines/min	*64 character type font

INPUT/OUTPUT EQUIPMENT CHARACTERISTICS

ANTICIPATED BY 1970

Table D-1

*Larger type fonts will be available at slower rates.

2.1 Incremental Magnetic Tape as a Replacement for Perforated Paper Tape

Perforated tape equipment was originally developed for use in connection
with land line data transmission and the performance characteristics
of the devices available were closely linked with the speeds of the lines
on which they transmit and receive. With the advent of high speed digital
computers, perforated tape reading equipment has been developed with
the capability of reading several thousand characters per second. However,
as the punching process is essentially mechanical in nature, involving
making physical holes in the tape, the best speeds attainable have been in
the order of 300 characters per second (slightly less information capacity
than is available on a 2400 bit per second line).

Although paper tape units with MTBF's in excess of 1000 hours are
more reliable than some other militarized peripheral equipment available,
they still require extensive operator attention. A 300 character per
second perforator consumes one 1200 foot reel of tape in slightly over
seven and one-half minutes; therefore, constant operator attention must
be provided in order to change reels.

The use of high speed tape perforators also entails a serious supply
problem since a tape perforator operating at full speed consumes non-
reusable tape at the rate of 13.6 pounds per hour at a typical cost of 60¢
per pound. Further, the tape itself is subject to deterioration through
aging.

In contrast, an equivalent size reel of magnetic tape contains 2400 feet.
When incrementally recorded at a density of 556 characters per inch,
the reel of magnetic tape is equivalent to 80 reels of perforated tape.
Thus, it allows much longer periods of operation without operator inter-
vention. Since the magnetic tape is reusable and has a life in excess of
20,000 passes, the supply problem is drastically reduced.

Present tape punching equipment has achieved reliability on the order
of 1000 hours MTBF; however, the equipment is essentially a highly
stressed, high wear item that requires one time use tape. Two inter-
mediate approaches can be taken to overcome limitations of present
tape punching equipment. Where human readability is necessary, the
perforated tape can be eliminated entirely as an intermediate machine
language and replaced by an alphanumeric printout captured directly
from the transmission line or another machine via a printer. This
printout may later be used as machine input by using character recog-
nition equipment. Advantages are gained in replacing the punching
mechanism by alphanumeric printing mechanisms which can operate
at higher speed and in allowing direct operator reading rather than
tape interpretation by "reading the holes." Since the printing can be
produced and read without mechanical action, highly stressed moving
parts can be substantially reduced. Non-impact printing and character
recognition are discussed in greater detail in later parts of this appendix.

Where no direct operator cognizance of data is required, perforated
paper tape systems may readily be replaced with incremental magnetic
tape systems in which data is recorded character by character on a
reusable magnetic tape in much the same manner that it would have
been on a paper tape. Since no electromechanical punching mechanism
is required, total system wear is substantially reduced which should
substantially increase input rates. The magnetic tape can be written
in the same language and format that is used on block read magnetic
tapes. Hence, this tape may be read directly into a computer system
at speeds much higher than are attainable with perforated tape
equipment.

Incremental magnetic tape recorders offer an improved technique
for the recording of synchronous and asynchronous, bit serial or

character serial, information.   They will be of primary value to the
Navy in communication and data collection applications.

Since incremental magnetic tape equipment records at a higher density
than perforated tape equipment (556 characters per inch as opposed to
10 characters per inch), the recorded data is much more transportable
and much smaller quantities of media are required.   The reusable nature
of the magnetic tape as opposed to the expendable nature of the perforated
paper tape offers a further reduction in the supply and storage problems.

2.2   Incremental Magnetic Tape Recorders

Existing commercial incremental magnetic tape recorders typically
use standard 2400 foot rolls of 1-1/2mil thick oxide coated Mylar
computer tape and are capable of recording data in IBM format at
densities of 200 to 556 characters per inch.   Recording is accomplished
while the tape is stopped under the recording head.   Non return to
zero (NRZI) recording is used since it requires only one incremental
tape advance per character recorded.   Also, NRZI recording is fre-
quently necessary in order to provide IBM compatible tape format.

After a character has been recorded the tape is advanced one 1/200
or 1/556 of an inch to the position where the next character will be
written.   This tape advance is usually accomplished by driving the
tape capstan with an incremental motor, or with a standard capstan
drive motor equipped with an incremental sensing device.

Since little energy is required for the tape drive, total power require-
ments of the recorder are low.   The slow tape speeds do not cause
rapid wear of the mechanism and therefore do not require high levels
of maintenance.   The unit is relatively inexpensive (about $3,000 in
quantity purchases, with electronics) and the magnetic tape is reusable and

can store very large amounts of data (approximately 12×10^6 characters per reel.)

Since incremental magnetic recorders are useful in the same functional applications as perforated paper tape punches, the two are compared in Tables D-2 and D-3.

The lower power requirements, long MTBF, and long recording time per reel of tape makes incremental magnetic recorders suitable for use in remote data collection systems in which perforated tape would not be suitable.

The high recording speeds which incremental magnetic tape systems can obtain, coupled with the long recording time available from a reel of magnetic tape, make them able to serve high speed communication lines much more effectively than paper tape. The two areas where perforated tape presently has an advantage over magnetic tape are in low-cost, low-performance systems and in systems where perforated tape is required for compatibility with other existing equipment.

Where a computer requires magnetic tape units for normal operation, it is possible to provide asynchronous off-line data collection by the use of compatible incremental tape. An off-line paper tape system would necessitate a paper tape reader on-line with the computer at extra cost.

In order to obtain high density recordings with reasonable size head gaps, bit positions are often overlapped during the recording process. See Figure D-1. This also allows the recording head to operate at more than one tape density.

Recording speed is dependent upon the ability of the tape advance mechanism to discretely advance the tape in increments of 1/200 of 1/556 of an inch and maintain a tolerance of $\pm$ 10% required for IBM compatible tape.

Current state-of-the-art is about 500 steps per second. This may be extended to 800 steps per second in the next several years, but advances beyond this are not predictable.

	Incremental Tape Recorder		Paper Tape Punching System (Current State of Art)		
	Current State of Art	1970 State of Art	High Perf.	Medium Performance	Low Perf.
Approx. Cost (No Control Elect.)	$3,000	$1,500	$10,000	$1,000	$500
Speed in Char/Sec	500	800	300	60	20
Density in Char/In.	556 (1/2" tape)	800 (1/2" tape)	10 (2/3 to 1" tape)	10 (2/3 to 1" tape)	10 (2/3 to 1" tape)
Cost of Tape per Char.	.0003¢	.0002¢	.0008¢	.0008¢	.0008¢
Is Tape Reusable	Yes	Yes	No	No	No
Max. Char/Reel in Millions *	9.6	14.4	0.12	0.12	0.12
Est. MTBF in hrs.	10,000	10,000	1,000	Varies	Varies Widely
Est. Power	150 w	60 w	400 w	120-250 w	100 w

* With 1000 Character Records

COMPARISON OF INCREMENTAL TAPE RECORDERS
AND PERFORATED TAPE PUNCHES

Table D-2

| ADVANTAGES OF INCREMENTAL MAGNETIC TAPE RECORDERS	ADVANTAGES OF PERFORATED TAPE RECORDERS
Lower cost for high performance unit.	Lower cost for low performance systems.
High recording speeds obtainable.	Provides permanent recording.
Reusable recording medium, e. g. lesser supply problem, lower cost per bit recorded, less operator intervention to change tape.	Produces tape that can be used by typewriters and other paper tape equipment.
	Visual inspection of output is possible.
Produces tape that can be used directly by computer tape transports.	
Lower power requirements.	
Longer MTBF	

ADVANTAGES OF INCREMENTAL MAGNETIC TAPE RECORDERS

AND PERFORATED TAPE RECORDERS

Table D-3

OVERLAPPED RECORDING
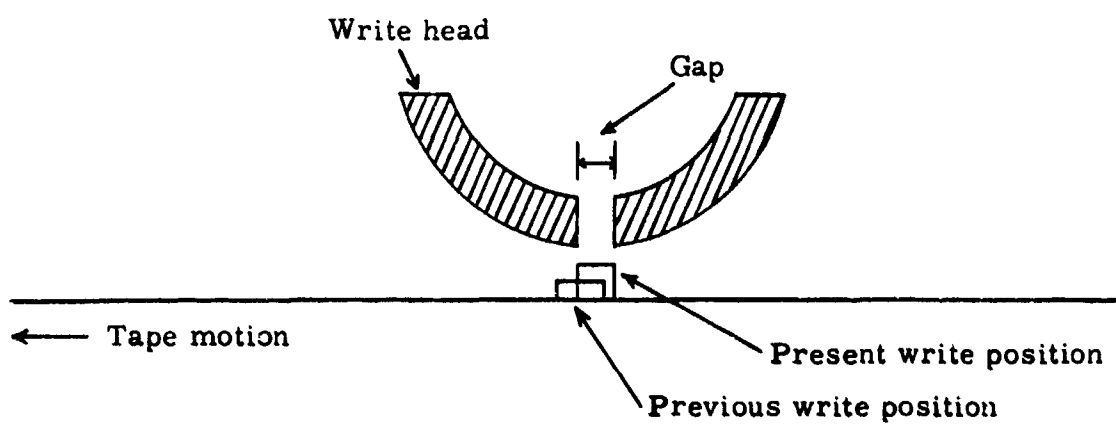
Tape advances .005" for 200 bpi recording density

Tape advances .0018" for 556 bpi recording density

Figure D-1

Maximum recording density is determined by tape standards that are based on limitations of tape reading techniques. Present techniques require an average space between bits of 1/200, 1/556, or 1/800 of an inch for IBM NRZI recording. They also require regular spacing of bits (e. g. , $\pm$ 10% tolerance for compatible tape.)

Current reading techniques can read NRZI recorded data up to 800 bits per inch; however, current incremental magnetic tape recorders are only able to maintain satisfactory bit-to-bit accuracy up to densities of 556 bits per inch because of limitations in incremental tape advance techniques. In several years, improvements in incremental motors will allow recording of densities of 800 bits per inch or more with the result that use of NRZI reading techniques will become the limiting factor in increasing bit density.

2.3 Incremental Magnetic Tape Readers

Incremental magnetic tape readers are similar in applications and mechanical design to incremental magnetic tape recorders. They are frequently designed to use the same tape transport mechanism; however, their principle of operation is different and their performance is limited by somewhat different parameters.
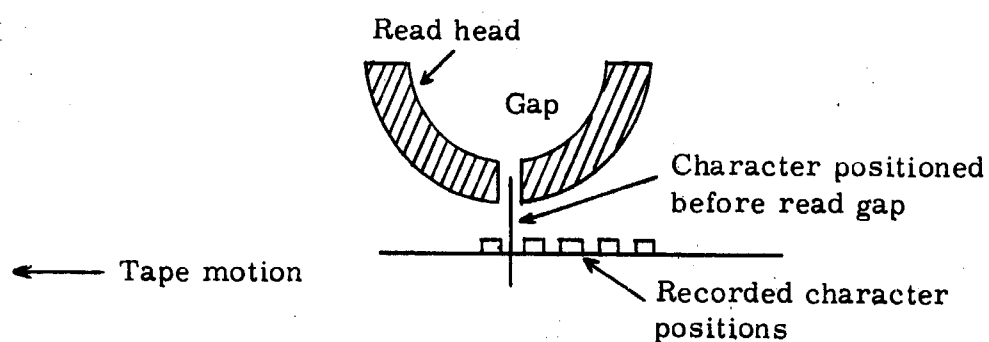
In most incremental magnetic tape readers, data is read by detecting a change of flux on the tape as it is moved across the gap of the read head. This requires that the tape be in motion when it is read. In order to supply this motion and yet allow synchronous access to each character, the tape is first accurately positioned in front of a recorded character and then driven into the character position to detect any flux change that may be present. The tape may be stopped while the character is still under the head and a second incremental step used to preposition the tape

prior to reading of the next character (see Figure D-2) or tape movement may be so controlled that only a single step is required. One manufacturer has produced an incremental reader that utilizes a flux sensitive head which allows data to be read while the tape is motionless.
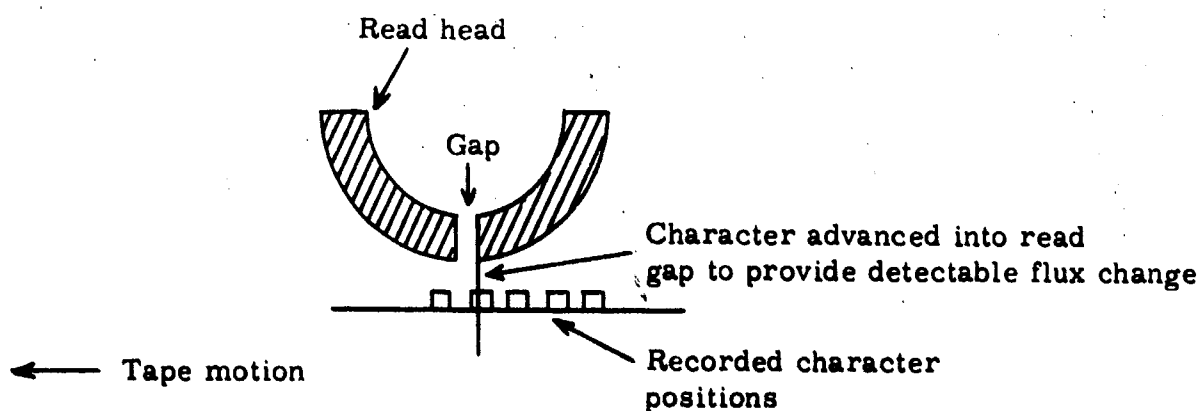
Since closer motion control is required to read each recorded character, it is not practical to incrementally read tape at as high bit densities or as high speed as those at which it can be incrementally recorded. Current state-of-the-art for reading is 300 characters per second at 200 bits per inch. This may be improved to 500 characters per second at 556 bits per inch during the same time period that incremental recording is expected to be improved to 800 characters per second at 800 bits per inch. Since incremental magnetic tape readers are useful in similar functional applications as perforated tape readers, the two are compared in Tables D-4 and D-5.

Table D-5 indicates that incremental magnetic tape readers do not offer all of the advantages over perforated tape readers that incremental magnetic tape recorders offer over paper tape punches.

Militarized versions of incremental magnetic tape recorders and readers that use a 300 foot cartridge of magnetic tape are currently available. Data is recorded in 200 bpi IBM format at up to 500 characters per second and read at up to 150 characters per second. These units are capable of meeting MIL-E-16400. The small tape cartridge and low recording density limits recording time to about six hours. This is far less than is obtainable by current state-of-the-art but far in excess of that which is practical with perforated tape.

Read head

Gap

Character positioned
before read gap

Recorded character
positions

Tape motion

Step 1.   Position of tape pre-positioned for reading
but before read step.

Read head

Gap

Character advanced into read
gap to provide detectable flux change

Recorded character
positions

Tape motion

Step 2.   Position of tape after read step.

TWO STEP TAPE MOVEMENT USED FOR

INCREMENTAL READING

Figure D-2

D-13

COMPARISON OF INCREMENTAL MAGNETIC TAPE READERS
AND PERFORATED PAPER TAPE READERS

	INCREMENTAL TAPE		PAPER TAPE SYSTEM (Current State of Art)		
	Current State of Art	Anticipated Future State of Art	High Perf.	Med. Perf.	Low Perf.
Appx. Cost	$4000	$2500	$5000*	$4500*	$650*
Speed in Char/Sec (Asynchronous)	300	500	1000	400	60
Density in Char/In.	200	556	10	10	10
Max. Char/Reel with 1000 Char. Record	5×10^6	11×10^6	0.12×10^6	0.12×10^6	0.12×10^6

* Commercial reader and tape handler combination

Table D-4

ADVANTAGES OF INCREMENTAL MAGNETIC TAPE READERS	ADVANTAGES OF PAPER TAPE READERS
Can read computer generated tape. (The computer can generate magnetic tape on line at 90 KC or more compared to 0.3 KC or less for paper tape.)	Available in a wide variety of cost and performance levels.
Can be readily combined with incremental recorder to provide dual purpose unit.	Higher reading speeds possible. Can read short piece of tape.
Tape is reusable.	Can read output of existing perforated tape equipment.
Can accomodate large amount of data due to high density of recording.	
Low power requirements.	
Long MTBF.	

ADVANTAGES OF INCREMENTAL MAGNETIC TAPE READERS
AND PAPER TAPE READERS

Table D-5

All incremental tape reading equipment presently available uses 200 bpi, 1/2 inch wide tape with IBM compatible format; however, current technology is suitable for the development of a cartridge-loaded incremental tape unit to read or record 1 inch wide, 450 bpi tape, compatible with the militarized digital magnetic tape transport model MT-451 developed by Sylvania under contract NObsr 87543.[1]

2.4 Non-Impact Printers

High speed electromechanical printers are normally used to provide printed output on computing systems designed by most computer manufacturers. They are an outgrowth of the punched-card tabulator and were designed for use in business applications where a number of carbon copies are required. Their speed, cost, and availability have also caused their adaptation as peripheral equipment on scientific and military computers.

Electromechanical line printers are presently capable of printing line lengths of 20 to 160 characters with type fonts of 64 characters at 1500 lines per minute. Within the next few years, speeds will probably be pushed up to 2000 lines per minute. Detailed discussions of various types of electromechanical line printers, their operation and functional limitations, are contained in Volume V, Section 2 of the ANTACCS Final Report.[2] Recent research in electromechanical line printers has been directed toward

(1) Use of belt, chain and horizontally moving stick printers in place of drum printers to reduce the cost of the type font and allow field changes in the type font. (A 64 character 120 column horizontal stick printer requires 184 characters of type while a 64 character 120 column drum requires 7680 characters).

(2) Time sharing hammers to reduce hammer and hammer driver cost. This is done by separating the type used for odd and even columns in a manner such that a hammer with a head two columns wide is first fired to print the odd columns and then to print the even columns. This technique allows 60 hammers and hammer drives to print 120 columns..

(3) Varying the presentation of each character to a line position such that all like characters in the same line are printed in sequence rather than in parallel. This reduces power supply requirements, and allows the printer to operate on line with a computer in a quasi character at a time mode without use or requirement for a line buffer.

Although electromechanical line printers are suitable for commercial and scientific applications, these printers suffer several disadvantages when used in a military environment including:

High maintenance requirements

Large power requirements

Large physical size

Heavy weight

Noisy

Recently, technologies for the implementation of non-impact printers have advanced significantly.[3] The non-impact printer has many advantages since moving parts are reduced to a minimum with resultant increases in reliability and decreases in power requirements. The major disadvantage of non-impact printers has been their inability to satisfactorily produce multiple copies.

The enhanced ability to produce inexpensive dry copies through processes such as xerography make possible major expansion in the non-impact

printer field. All previously developed systems using impact printers have been designed to produce the maximum number of carbon copies required for any application. These are printed at one time in the printer and distributed in accordance with some fixed pattern designed to accommodate the "worst case" condition for paper copy requirements. In most systems, many of the carbons are never used and represent a load on the preparation system, the distribution system, and the receiving system.

From a system standpoint, the ideal printer would have the capability of producing the exact number of carbons required under computer control, printing on each copy the destination to which that copy is to be delivered.

Current technology is developed to the point where this can be achieved by several techniques. These include use of an on-line printer to provide multiple printing of a single page with identified distribution for each copy and the use of an on-line printer to prepare a single page original which incorporates a bar code that can be utilized by an automatic reproducing machine to prepare the proper number of copies of each page. The latter system, if so desired, could select the color of paper on which each copy is to be reproduced to control distribution. The greatest bottleneck has been the restrictions which the systems designer has placed on himself through the utilization of existing and available high speed impact printing equipment. This has resulted in the slowing down of the development of non-impact printing equipment, and thus has not allowed effective development of new paper handling systems.

Techniques for non-impact printing examined in this study include electro-optical, electrographic, magnetic, electro-chemical, photo-chemical and ink spray printing. Table D-6 shows a comparison of these systems.

	Electro-Optical	Electro-Graphic	Magnetic	Electro Chemical	Photo-Chemical	Ink Spray
Typical Source of Character	CRT	Conducting Wires	Magnetic Type or Heat Source (Reverse Process)	Conducting Wires	CRT	Deflected Ink Spray
Direct or Indirect Printing	Direct/Indirect	Direct	Direct/Indirect	Direct	Direct/Indirect	Direct
Multiple Copies Possible With Single Exposure	No	No	For Indirect Process	Yes	For Indirect Process	No
Special Paper Required	Yes for Direct No for Indirect	Yes	No	Yes	Yes	No
Feasibility	Exists	Exists	Good	Exists	Exists	Exists as Character Printer

COMPARISON OF SELECTED NON-IMPACT PRINTING TECHNIQUES

Table D-6

The electro-optical technique utilizes an electronic-to-optical transducer such as a cathode-ray tube to form a character shaped optical output. This output is projected on a charged surface which is developed by dusting, spraying, or otherwise bringing the surface into intimate contact with a series of finely divided particles that are attracted to the surface in the charged areas. Unless a treated paper with high dielectric properties is used, it is then necessary to transfer this powder or "ink" to the final printing surface. In either case, the image is usually fixed in place by heating.

The electrographic printer makes use of a treated paper with high dielectric properties. As the treated paper is moved across a matrix of conducting wires, the paper picks up an electrostatic charge in the shape of the desired characters or symbols. The paper is developed by dusting, spraying, or otherwise bringing the surface into intimate contact with a series of finely divided particles which are attracted to the surface in the areas of the charge. This powder or "ink" is then transferred to the final printing surface and fixed by heating.

Magnetic printers utilize a shaped magnetic field formed by a magnetized type wheel, matrix, or stylus to form a character on a readily magnetizable surface. This surface is then used to transfer a finely divided magnetic material to the surface of the paper for heat development.

The electro-chemical printer uses a chemically treated paper which, when exposed to an electric field, reacts to form a localized blackening of the paper surface. Two versions of this technique are currently being investigated. In the first version, the heat generated by the electric charge is used to create a thermal reaction with the surface of the paper. Typical of this type of paper is that used in electrocardiograms and other hot stylus recorders. In the second version of electro-chemical printing, the voltage supplied by the print head is used to penetrate a dielectric separating two chemical compounds which react through the pinhole break in the dielectric to produce a visible output.

The photo-chemical electronic printer utilizes a photosensitive chemically treated paper much like a blue print paper. The chemicals used are slow reacting except in the presence of ultra violet light. The paper is subjected to a mild ultra violet exposure in the form of the desired characters produced by a fibre optic insert in the face of a cathode-ray tube utilizing an ultra violet phosphor. Invisible or latent images are produced on the paper which are then developed by further exposure to moderate ultra violet radiation. Unless the paper is fixed, continued exposure to light will gradually cause the background to darken so that printing will eventually become unreadable.

Ink spray printing utilizes a fine spray of fast-drying ink directed against a roll or sheet of paper. In present technology, the ink source is moved horizontally across the paper to determine character position and the ink is electrostatically deflected in order to "draw" characters. The principle used is much the same as that achieved in a cathode-ray tube by the electron beam being deflected to draw characters on the face of the tube. The number of moving parts required for a spray printer is reduced to an absolute minimum and includes only the paper transport, which is required for all printing devices, and the spray positioner.

In the future, it should be possible to develop a spray printer in which the ink is sprayed through a shaped opening in order to provide a conventional character shape rather than a "drawn" character. This could be achieved by spraying the ink through a character shaped opening in a moving bar, belt, or drum and releasing ink in synchronization with the position of the selected character opening. It could also be achieved by deflecting the spray through a selected opening in a fixed matrix, much as is done with the electron beam in a "charactron" tube. Although still early in development, ink spray printers seem to be one of the more promising approaches to non-impact printers.

From a technology standpoint, all non-impact printers utilize two subsystems of interest. These are the electrical to visual image transducer and the image developing technique.

The electrical to visual character transducer is usually a cathode-ray tube, a matrix of conducting wires, or an electro-static deflection system. In current printer implementations the cathode-ray tube is the only means of obtaining a high quality image. Unfortunately, these devices require high voltage which is not amenable to use of batch-fabricated circuits and solid state technology. The same holds true for the wire matrix and ink spray techniques as they depend upon a high voltage output either to generate a spark, heat, or an electrostatic charge. Switched beam laser technology which has been examined in the display section of this report offers an interesting candidate to replace the CRT or wire matrix, but relatively high voltages may still be required.

The image developing problem is one of major consequence in non-impact printers since most image developing techniques are not well suited for a militarized application.

With electrostatic, magnetic, and ink spray techniques, a material is deposited on the printing surface and then fused or bonded or evaporated in place. These techniques are probably the most suitable for military environments in that they add a material to the surface of the paper so that the paper can not be accidentally or intentionally altered by exposure to ultra violet light, chemicals, electromagnetic forces, etc.

The chemical developers utilize a chemically treated paper and either a gaseous development such as ammonia or a liquid developer. Development time is of considerable importance, fairly expensive equipment is required, chemicals must be frequently changed, and a supply problem is created. This type of development provides a fixed, unalterable, permanent copy, but it is bulky and cumbersome to use.

The self contained chemical reactants which are released by exposure to heat, ultra violet light, spark puncturing, etc. require a relatively expensive chemically treated paper and the copy can later be altered. Further exposure to heat, ultra violet light, etc. can permanently damage the copy to such an extent that it is useless. Therefore, an aging problem exists in the use of such papers. This class of material is generally not suitable for military applications.

2.5 Punched Card Replacements

The unit record or punched card is the least amenable of all peripheral equipments to developing into a solid state unit. Its very function requires that a small block of information be physically separable from other similar blocks of information so that it can be removed, replaced, or transported. In many applications, it is necessary that the unit record be legible to the human as well as to a machine. The nature of the unit record therefore requires that it be moved into a reader one record at a time and removed from the reader one record at a

time requiring some mechanism for this implementation. Current punched card readers approach their ultimate in possible simplicity as unit record devices in that their only moving mechanisms are those used to transport the card while reading through the use of solid state sensors.

Punching on the other hand represents a great problem area in that not only must the card be moved as in the reader but it must be moved one column or row at a time and stopped at each punch position. Dies must then be driven through the card cutting the paper to close enough tolerances to allow efficient reading. Over the last ten years, a number of approaches have been taken to eliminate the card punching problem. These include blowing out the chad with compressed air, burning out the chad, printing the card and reading the spots, replacing the card with a magnetic card, etc.

Since the card punch represents a weakness in the system, the two most appealing ways of improving it have been either replacing the punched card with a printed spot or using a magnetic card. The printed card offers some advantages in terms of cost and simplicity in that it can use inexpensive card stock but offers the disadvantages of having the code readily obliterated through abrasion, smudging of inks, dirt, etc. This may be partially overcome through the use of fluorescent dyes rather than inks.

The magnetic card, though considerably more expensive than the printed paper card, offers the possibility of reuse thus lowering effective cost. However, like magnetic tape the magnetic card is subject to data loss resulting from heavy magnetic fields. An interesting approach to the problem of a militarized card punch has been offered by Sylvania through the introduction of SMART. This is a system that uses oxide coated paper cards which are permanently recorded by an indenting quill. This system requires special cards which are not reuseable. It requires electromechanical indentation of the card which, though more complex than magnetic writing, is

simpler than card punching (and about equivalent to card printing). It provides a permanent record which can be destroyed only by destroying the card. Data can be recorded at considerably higher densities than can be achieved on a punched paper card thus partially compensating for the increase in material cost.

Since the punched card represents an intermediate document between the originator and the system, the best approach to militarization of the punched card may be its elimination or replacement. In the case of man originated data, use of character recognition equipment with constrained hand printed characters could not only eliminate the punched card, but also the card punch, the card reader, the keypunch, the keypunch operator and the errors that the keypunch operator makes in transcribing from hand written material to punched cards. In the case of machine generated data, data may be captured at its source in some form more suitable to the military environment such as an incremental magnetic tape or an on-line keyboard/display console.

2.6 Graphic Input Devices

Light Pens

When a light pen is used as a graphic input device, the display update rate is limited to about 8 us per point to allow enough energy transfer from the electron beam to the phosphor to activate the photo cell in the light pen. In some applications, this is a serious limitation on the total amount of information that can be displayed.

The "beam pen"[4] is a graphic input device that can be used to replace the conventional light pen without imposing limitations on the total amount of data displayed.

The beam pen is a conducting probe that is capacitively coupled to the front of the CRT screen in a manner such that as the distance between the beam

and the probe is decreased, the beam to probe capacitance and thus the
probe signal increases. Coincidence of the CRT detection beam and the
pen point can thus be sensed and the position of the pen point can be de-
termined by strobeing the CRT's horizontal and vertical deflection with
the output of the beam pen.

At the current state of development, the beam pen has a "field of view"
of 1.5 inch diameter. This is about 10 times that of current light pens
and too large for practical applications. It is doubtful if the field of view
of the beam pen can be reduced to that of the light pen since the activating
function of the beam pen has a slower attenuation rate than that of the
lightpen.

If the problems of poor resolution of the beam pen can be overcome, the
beam pen offers the advantage of increased response speed and freedom
from background noises that result from ambient room lighting in light-
pen systems.

The RAND Tablet

The RAND Tablet consists of a thin insulating sheet on one side of which
is an array of etched copper lines in the X direction and, on the other side,
a similar array of lines in the Y direction.[5] Capacitor encoding networks,
etched on the same sheet, are used to distribute a unique pulse train to
each X and Y line from a common pulse pattern generator. The pen con-
sists of a capacitive pick-up connected to a high input-impedance amplifier.
The pulse pattern received by the pen varies with the X and Y lines nearest
the pen tip. This bit pattern is translated into a binary representation of
the X and Y coordinates of the pen location by a code converter. The
system provides high resolution, is inexpensive, can be used with over-
lays, is semi-transparent so that it can be placed in front of a display,
and can be produced in large sizes.

A commercial implementation of the Tablet is currently available that offers a 10" x 10" drawing surface with a resolution of 100 lines per inch at a cost of less than $10,000. This unit has an operating range of 0° to 50° C. It measures approximately 20 x 24 x 1-1/2 inches and weighs 7 pounds without electronics. The electronics occupy 7" in a standard rack, weigh 35 pounds and draw 40 watts power.

The RAND Corporation is currently developing a large size tablet with a 32" x 32" active surface, and a resolution of 128 bits per inch or a total resolution of 4096 bits on both the X and Y axis. Over-all size of this unit is to be less than 50" x 50".

The drawing surface of the Tablet is said not to create or be sensitive to radio frequency interference.

In large sizes, perhaps with reduced resolution, the Tablet can be used with a pen pointer as a part of a large screen display system to allow direct graphic input from the surface of a large screen display system.

2.7 Digital-to-Analog Convertors

The digital-to-analog convertor is designed to convert a digital number to an analog voltage representation of that number.[6] A digital number is held in a flip-flop register which is connected to a resistive divider network. Resistances of the network are weighted in accordance with the assigned values of each bit position in the register. With a precision voltage supplied across the resistance network, the output voltage will vary with the quantity of the digital number heid in the register.

Factors controlling accuracy of digital-to-analog convertors are the tolerance of the individual resistance elements in the resistor network, accuracy of the reference voltage supply, and the number of resistance steps or

discreteness used. Application of hybrid discrete thin-film circuits to digital-to-analog convertors should offer substantial advantages in improved accuracy and reduced cost since the passive components may be made cheaply with tightly controlled tolerances and since there is no interaction between the active components. Batch-fabrication techniques are feasible for hybrid discrete thin-film circuits. Therefore, substantial cost reductions are possible in volume production.

2.8 Analog-to-Digital Conversion

The analog-to-digital convertor usually consists of a digital-to-analog convertor and a comparator.[7] The comparator compares a known output from the digital-to-analog convertor with an unknown analog voltage. Feed back is provided from the comparator to the flip-flop register of the digital-to-analog convertor and is used to increase or decrease the value held in the register until the output voltage of the digital-to-analog convertor matches the unknown voltage. When a match is achieved, the comparator provides a read strobe to indicate that the voltage represented by the value held in the flip-flop register has been equalized with the unknown analog voltage.

Many variations of feed back are used to control the value of the reference voltage, each having its own advantage in terms of sampling rate, sampling time accuracy, conversion time, and cost.

Factors controlling the accuracy and cost of analog-to-digital convertors are similar to those determining the accuracy and cost of a digital-to-analog convertor and similar improvements in cost and accuracy can be anticipated in the future.

3 DEVELOPMENT OF NEW TYPES OF INPUT/OUTPUT EQUIPMENT THAT
    ARE NOT IN WIDESPREAD USE AT PRESENT

Several new types of input/output equipment are under development that

offer promise for performance improvements in future systems. These
include:

> Character recognition and print readers
>
> Voice input and voice output
>
> Non-mechanical keyboards
>
> Solid-state replacements for magnetic tape equipment

Some of these, such as optical character readers, are in limited use at
present while others, such as voice recognition equipment, are probably
ten years or more away.

The term character recognition is applied to a broad range of applications,
from relatively simple ones such as reading small fonts of highly stylized
magnetic ink characters on bank checks to reading hand printed characters
and fifteen or twenty different type fonts on non formated documents. By
1970, equipment will be available which is capable of reading typewritten
characters at rates of 2000 to 3000 characters per second with reject
rates of less than 0.005% and misreads of less than 1 in 500,000. The
same or similar equipment should be able to read multiple type fonts and
constrained hand printed characters at somewhat reduced reading rates.

Advances in integrated circuit logic components and memories discussed
in Appendices A and B will provide significant reductions in cost since
the implementation of character recognition equipment involves complex
logical functions.

Research into voice recognition and voice output techniques is being
supported in a number of organizations at this time. Limited voice out-
put equipment is now available and in use that is capable of assembling
recorded words or syllables into a message. Equipment for truly synthesi-
zing voice output from digital information is also available, but it is more
expensive than word assembly techniques and requires greater storage.

Equipment for recognizing spoken messages as computer input is in fairly early stages of research and it is too early to predict any cost and performance characteristics for devices of this type.

Keyboards have always played an important role as a man to machine-language transducer. This is true both of off-line data preparation devices, such as keypunches, and of real-time data input devices such as display consoles which provide man-machine interaction. Present types of electromechanical keyboards have suffered from reliability problems and have required the user's fingers to operate in a basically flat rectangular area. New types of keyboards are being developed that do not involve mechanically moving parts and that may permit more design freedom from the human factors standpoint. These include pneumatic, optic, and piezo-electric techniques.

Solid state replacements for magnetic tape may improve the speed and reliability available for this type of input/output function, however, they may prove to be more costly devices than magnetic tapes. At least two different programs are underway to develop solid-state storage modules that could be plugged into read-write electronics in a manner somewhat equivalent to placing a reel of tape on a tape unit. If this proves feasible and reasonably economical, the input/output and off-line storage functions presently provided by magnetic tape could be provided by high-speed, high-reliability devices and media with no moving parts.

The goals for one development program of this type (BORAM) are 4 million characters per module, read-write rates in the order of 2 or 3 million characters per second, and costs of approximately 0. 015¢ per character for off-line storage.[6] A further advantage that would be offered by this particular device is random access (in 1 usec) to any

block of data within a storage module. This is in contrast to the serial access required by magnetic tape. The read-write unit would have approximately 1/10 the power requirements and weight of a magnetic tape unit and about one half the size. If a device of this type provides random access to a block of data in the storage module, it could also be used as a replacement for electromechanical on-line mass memories such as magnetic discs, magnetic drums, and magnetic card files.

3.1 Character Recognition and Print Readers

Character recognition is most frequently used commercially in applications where data has been created at a central point, distributed to a number of points for later human use, then returned for subsequent computer processing. When data is intended for human use it should be written in a human-readable language. When it is also required for later computer processing the use of character recognition will allow the reuse of the same data without intermediate keypunching or other transcription.[9] There are a number of other means which could accomplish this purpose. These include magnetically recorded information on the back of a printed form such as is used on bank ledger cards; punched cards which carry both the punched holes and a printed interpretation of those holes as used in utility bills; and bar coding schemes which include both a bar code suitable for easy machine reading and characters which are suitable for human reading. The latter are frequently used on oil company credit cards.

Character recognition can be used for entering data that was previously created for human use only (e.g. books, reports, etc.). In this type of application, character recognition equipment has frequently been considered as a data input source for computer operated language translation systems.

Character recognition equipment is also useful in applications where documents are created from a large number of widely dispersed locations for entry into a central data processing system. In this type of application the cost of installing equipment to provide machine coded data at each of the remote locations can become so high that it is more economical to install a small inexpensive printing device and rely on a centralized character recognition system to convert to computer input. As character recognition equipment becomes available to read constrained hand printed characters, it will be applied to this use, since this will eliminate the need for any remote coding or printing device.

Some of the applications discussed above are not found in the present NTDS but are likely to occur in more general tactical data systems — particularly if intelligence reports are involved. Marine Corps data systems may utilize this type of equipment for entering typed or hand printed data originating from small remote field units.

Attempts to develop character reading machines have relied on a wide diversity of technologies; however, recent work has centered around three general techniques. These techniques are mask matching, feature matching, and matrix matching. Each of these techniques has been incorporated into one or more pieces of usable character recognition equipment. Each has its own advantages and its own limitations and is, therefore, applicable under certain conditions.

Mask matching consists of comparing the character as a total entity with a standardized version of the character in order to determine whether the two are identical. Mask matching may be done either optically or electronically. In either case, it is done by comparing

one shape with another to determine identity. In the typical optical system, the character to be identified is projected against a series of negative masks. Where there is no match of the character, light passes through the mask and can be seen by a photo multiplier. Where a match exists, the dark area of the character obscures the light area of the mask causing a minimum light transmission which is detected by the photo multiplier and is used to identify the character. Since some large characters can completely obscure a small character (e. g. an L could obscure a period) both a positive and negative mask are usually used, and coincidence of maximum and minimum light output determines the identity of the character. In order to compensate for variations in skew and alignment, the projected character is usually optically rotated and vibrated during the time in which it is matched against a mask.

This same technique is used electronically by matching an electrical signal generated by the read head against a set of standard electrical signals (masks) which represent each possible character match.

Optical mask matching in theory is an attractive means of character recognition since the masks can be built quite inexpensively — all logic is optical, and only the recognition circuits are electronic in nature. Unfortunately, a large number of masks are required for any appreciable type font size, e. g. a 64 character type font would require 128 masks. Further each variation of a type font used must include its complete set of masks as the machine is recognizing a specific shape including all its characteristics rather than selected characteristics that could be common to a group of characters from similar fonts.

If a reasonable reading speed is to be obtained, the character must be projected against all possible masks at the same time.

This involves an elaborate and complex optical system with its result-
ant attenuation of light. The more characters that must be read the
more extensive the optical system and the greater the light attenuation.
This attenuation can only be overcome by a high intensity light source
with the result that light reflection is usually not adequate and the
printed source must be on film for projection. Hence, what started
out to be a simple and inexpensive system frequently becomes a very
complex, expensive system. The state of present technology for op-
tical mask matching is such that it could be developed into a small
system for reading a specified set of numeric characters, or perhaps
alphanumerics, but it is not suitable for multiple font readers or the
reading of any printed matter except that which has been prepared
under a specially controlled condition.

Matrix matching is similar in theory to mask matching. However, it
is dependent upon the point by point matching of a character against
its match rather than matching the character in toto. The system
operates by scanning a character point by point and storing the light
value of each point in a recognition matrix. The size of the matrix
varies with the refinement of the system; however, it usually con-
sists of several hundred points. Each point is identified as to its
color, e. g. black, dark grey, grey, light grey, or white. When the
character has been completely entered into the recognition mask, it
is moved horizontally and vertically into a standard position and ro-
tated to match a base line.

In some systems, the character is then expanded or contracted in
order to fit a given recognition area of the matrix. In other systems
this is accomplished optically before entry of the data into the matrix.
The recognition matrix is then matched against a series of character
matrices in order to determine identity. Since no printed character

is perfect in its composition (e. g. voids, fuzzy edges, and other variations will occur from one character to another), the recognition matrix determines the probability of a character occupying each area of the matrix and the relative grey factor of each area. It is not necessary that the character be perfect, but rather that it come within some percentage match of the character matrix. A number of character recognition machines have been constructed using the matrix matching technique.

Matrix matching has proved to be a suitable and practical technique for reading both single and multiple type fonts. Closely related type fonts can be read using the same character masks and in many cases it is possible to allow a new font to be added by providing masks for only those characters that show substantial variation from one font to the other. Since this is essentially an improved mask matching technique, it is necessary to provide different character masks for each character of widely divergent fonts. Therefore, this type of system is not too practical where it is desirable to read a large number of widely different type fonts, hand-printed characters, or constrained handwriting. The limiting factor on the number of characters that can effectively be read is the electrical attenuation that results from driving the number of masks that must be provided. The larger the number of masks, the greater is the amount of power that must be used.

Feature matching is perhaps the most promising approach to a generalized character reader. Feature matching relies on scanning the character to detect certain pre-established features and matching these features against a series of truth tables representing each character...

The features that may be examined for character identity are determined by the particular design of the system. Features that have been used in the past have included determination of horizontal and vertical bars in the character, determination of line intersections and angles of line intersection, number and position of closed loops; number, position and direction of opening of open loops; number and position of line ends, etc. The criteria used can be reduced or expanded as required by the number of type fonts that must be read. Since many characters from different type fonts have the same features in common, feature matching systems are readily upgraded for multifont reading. They have also been used experimentally with some success to read constrained hand-printed characters.

Feature matching is the most suitable system for recognition of hand-printed characters. As an example of its capability, in September 1962, 100 students at Tufts College were given thirty minutes of instruction in hand-printing numerals. They were then asked to produce copy for character recognition equipment utilizing feature matching. Of 56,000 numbers produced, only 120 were rejected as non-readable.[10]

In summary, the current state-of-the-art of character recognition of printed and constrained hand-printed characters is such that usable equipment can be made available for use in 1970 era Navy systems.

3.2 Voice Input

Voice input to a computer system involves two major functions — speech recognition and word interpretation. Speed recognition is the analysis of the human voice in order to determine phonetically what word is spoken. Word interpretation is the differentiation of one spoken word from other similar spoken words and synthesis of its alphabetic rather than phonetic equivalent for use as computer input.

Most of the work in voice input has been concentrated in the areas of speech recognition. The problems involved in speech recognition are similar in nature to those encountered in character reading. In both cases it is necessary to analyze the input into a series of identifiers that are then compared with a set of standard criteria to establish input identity. In voice recognition systems, extensive variation in input occurs as a result of differences between voices from individual to individual and because of the variations of the voice of a single individual over a period of time. Aging causes gradual long term variations in the frequency output of vocal cords; minor physical conditions (e. g. colds, sinus trouble, etc.) cause considerable variation of a speaker's voice from day to day; and the emotional state of the speaker varies from moment to moment with a resulting variation in emphasis on each word spoken which varies the relative frequency distribution and power distribution of the spoken word.

While a character recognition system can be useful if it can read a font of 64 characters, a generalized speech recognition system must be able to accept several thousand words. Speech recognition systems must deal with a group of variables in pitch and intensity that are occurring over the period of time while the word is being spoken; however, character recognition systems can evaluate all of the criteria for one character at a single moment in time. Since the length of words also varies greatly, it is necessary to determine both the beginning and ending of a word in order to provide its complete analysis.

Contextual interpretation seems to be a frequently ignored facet of the voice input problem. This is probably because the problem of speech recognition is so far from solution. However, if a satisfactory means of voice input to a computing system is to be achieved, this

problem must also be solved. Voice identification systems are faced with the problem of determining word meaning, but they must determine meaning not only for words of different meanings that are spelled alike, but also for words that sound alike but are not spelled alike. They must recognize syllables of words as a partial word rather than a whole word. For example, they must be able to distinguish the following:

> I have <u>four</u> apples.
>
> They are <u>for</u> you.
>
> We played in a <u>four</u>some. .
>
> The word is <u>for</u>eign to me.

In each of these examples, the word "for" sounds the same, yet could not be treated in the same manner within a computer. Voice recognition equipment capable of recognizing the word "for" is still not a useful device until it is able to distinguish true identity — e. g. whether the input should be transmitted to the computer as a digit, a word composing part of a sentence, or a syllable comprising part of a word. Word meaning is not an insurmountable problem, but it is one that will require considerable effort before a solution is available. At present insufficient effort is being devoted to this area of voice recognition.

3. 3 Voice Output Equipment

Voice output equipment, intended for on-line use with a computer, is currently available from several manufacturers. Response speed, output rate and vocabulary are limited primarily by economic rather than technical considerations. Voice output systems allow the use of inexpensive telephone equipment as computer inquiry devices and eliminate the need for modems (digital-to-analog and analog-to-digital convertors) on each end of the telephone line.

In a typical system, a touch tone (10 key push button tone activated dial) telephone is used to call the computer.[11] Both the computer and the calling phone are connected via a conventional telephone exchange system. The computer acknowledges the call vocally and asks the user to enter his request. The user enters his request via the touch tone dial, the computer processes the request, composes a vocal reply and issues it to the user. This type of system is presently in use to provide stock market quotations and for airline reservation systems. The economic advantage in the use of voice output equipment is that it eliminates the need for specialized remote terminal input/output equipment and modems.

In a real-time system voice output can be useful as a means of issuing instructions to an operator and as a means of sounding oral alarms. Voice output is particularly advantageous where the telephone system or other audio communication systems are already in existence since it allows the computer to communicate over this network without the installation of additional peripheral equipment. Unlike the traditional means of visual output from a computer, voice output is able to alert the operator under any circumstances including periods of time when his attention is elsewhere, when his back is turned, when he is in an adjacent room, or even when he is asleep.

Several types of voice output equipment are currently in use. One type of equipment is a peripheral device that stores recorded words or "canned messages" that may be called up as output under computer control. Words are recorded in analog fashion usually one to a track on a drum or tape-loop system. They are switched into the output circuit of the voice system as the computer selectively activates the magnetic read heads. Such systems are limited in output capacity by the number of tracks of audio storage which are available. One such system that is commercially available has a maximum capacity of 128 words.

Another type of system utilizes conventional digital storage techniques to store digitalized versions of each word. These are called up as required and passed through a series of filters with suitable energizers. An audio output is obtained by the combination of the output of these filters which are selected by a pattern of input data. In such systems, coded voice can be stored in the same type devices used by the computer to store digital data including disc, drum, card, magnetic tape, or punched paper tape. In one commercially available system of this type, fifteen filters are used to cover the voice frequency range of 200 to 3700 cycles per second.[12] Approximately 2400 bits of storage are required for each second of voice output or 800 bits per word at an average speaking rate of 180 words per minute. The number of words that can be stored in this type of system is limited only by the availability of computer memory and on-line auxiliary storage that is accessible within the time delay permissible in creating the output message.

In both types of equipment the output message is at least partially preconceived and recorded as a series of numbers representing the addresses of the words or syllables to be selected. In some equipments the output selected is based upon the input of a request to the system. For example, the user requesting a stock quotation provides an input of the symbol of the stock in which he is interested. This symbol in turn is used to provide an address at which the last stock transaction is stored. This is then used to select the audio equivalent of numbers representing the value of the last transaction.

Voice output offers a number of advantages for advanced tactical data systems — particularly for the dissemination of computer output messages over normal voice channels to remote units. A militarized version of present commercial equipment could be implemented on a relatively short schedule. Since the versatility of current techniques

is dependent largely upon the storage available, voice output in the future will be more a storage problem than an input/output problem.

3.4 Non-Mechanical Keyboards

The keyboard has been the major means of man-to-machine communication since the introduction of data processing equipment, but little has been done to improve keyboard mechanisms. There are many technologies which can be applied to the creation of a non-mechanical keyboard as a replacement for a mechanically encoded keyboard. In commercial applications there is little incentive to develop new types of keyboards since contact closures have proven to be sufficiently reliable for normal office conditions. However, in highly corrosive atmospheres, explosive atmospheres, and areas of environmental extremes, improved keyboard techniques are needed. Non-mechanical keyboards offer definite reliability and maintainability advantages under the type of conditions in which the Navy system must operate. Other human factors type advantages are also achievable.

Computer input keyboards are essentially mechanical to electrical transducers coupled with some form of encoding device. Presently, the encoding is either mechanical or electronic. Most existing keyboards depend on some form of mechanical contact closure for the mechanical to electrical transducer and utilize one of the following forms of encoding:

> Direct contact (or uncoded)
> Direct code generating
> Matrix coded
> Serial coded

Direct contact or uncoded keyboards utilize a key which is connected directly to a switch so that activation will cause a contact closure.

Output is an open or closed circuit which may be used directly or used in conjunction with a code generator to provide coded output. These keyboards require at least one contact for every switch or key, and at least one wire connected to each contact plus a ground wire.

In directly encoding keyboards, each key is linked to a mechanism that allows a number of contact closures to occur at the same time. The group of contact closures allowed varies with each key and this provides the direct generation of an output code. Although mechanically more complex than uncoded keyboards, the number of contact closures can be substantially reduced as can the number of data transmission lines. One contact closure and one line plus a ground is required for each encoded bit generated.

The matrix encoded keyboard is, in effect, a key activated crossbar switch. Each key is connected to a cross point so that depression of a key will close a contact representing the row in which the key is located, and a contact representing the column in which the key is located. Matrix encoded keyboards require one switch and output wire for each row and each column position.

Serial coded switches provide a unique bit serial code output for each key. Each key is connected to a device (usually mechanical) that generates a series of identifying timed pulses. This type of output is particularly advantageous in applications such as transmission over telephone or teletype lines.

In military keyboards it is desirable to reduce mechanical actions and contact closures to a minimum.[13] It is possible to eliminate contact closures in the previously described devices by replacing them with some non-contact form of mechanical to electrical transducer, e. g.

magnetic transducers, optical transducers, piezo-electric transducers, and capacitive transducers. The transducer is then used to generate a pulse that is used to trigger a flip-flop. The flip-flop provides output such as a contact closure.

There is little generalized keyboard technology in the sense that there is a memory or circuit technology, since each keyboard is designed for some special application and the method of implementing the encoding or contact closure is usually left to the keyboard designer. The following examples illustrate ways in which the previously mentioned types of transducers can be used to provide various solid state keyboard configurations.

A direct contact keyboard or uncoded keyboard can be implemented with piezo-electric crystals by coupling a crystal directly to each key so that pressure applied to the key is transmitted to the crystal resulting in an output voltage. This pulse can be used to set a flip-flop which provides the equivalent of a contact closure. No mechanical key movement is required.

A directly encoded keyboard can use multiple piezo-electric crystals to generate a coded output for each key directly. This output could either be parallel or serial. Other techniques that can be used for direct coding of output eliminate contact closures but involve some minimal amount of mechanical motion. These include keys which interrupt light beams directed at photocells, keys which move a permeable material in a magnetic field to generate flux changes, and pneumatic keyboards in which the fingers cover openings through which air under slight pressure is normally escaping. In a pneumatic keyboard the change in backpressure caused by placing a finger over one of the openings is sensed and can be used to actuate pneumatic logic to

generate a coded output. Optical keyboards are available in which no mechanical contact closure is required. In these devices, key movement either interrupts or creates a light path that directly encodes the character on photocell receptors. In some of these approaches (e. g., pneumatics) the absence of mechanical linkages can permit greater flexibility in the human factors design of the shape of the unit and the placement of "keys".

The light pen is another interesting keyboard replacement for certain applications. Typically, with a CRT display console, a series of selections or choices can be presented to the operator who can identify one or more with a light pen. [14] (The choices offered to the operator could be the letters of the alphabet.) On the basis of the initial selection, certain data is processed and a new set of choices are presented to the operator. Machine and operator thus work their way through a complex set of machine-aided man-made decisions based on rapid access to the large amount of computational power and reference data available in the computer. The display and light pen thus act as a computer modifiable selection matrix which can provide the man-machine interaction so important to a real time system.

3.5 Solid-State Replacements for Magnetic Tape Equipment

In the present NTDS, magnetic tape is used primarily for the purpose of program storage. In this application program tapes are kept on line with the computer to allow re-entry of a program in case of computer failure and to allow fast changes in computer functions by entering a new program from the tape.

Future applications of magnetic tape in NTDS type systems may also include:

> Temporary storage of intermediate results where it
> is not economical or practical to furnish sufficiently
> large main memory.

A media for transferring data from one system to another
in the same or different physical locations.

Off-line storage of data not required for the immediate
problem.

The wide range of applications for which magnetic tape storage is suit-
able is largely the result of the characteristics of the tape rather than
the tape transport.   These desirable tape characteristics include:

Low cost per character of storage.

High density of storage.

Light weight of the tape in terms of characters per pound.

No power required while data is in stored condition (i. e. not
being read or written).

Read/write speeds that are relatively commensurate with
the speeds of computing systems.

Reusable over a prolonged period of time with negligible
wear or degradation.

Some commercial equipment can provide much higher peak transfer
rates, but presently available militarized magnetic tape units provide
comparable overall performance since the overall performance is
limited by start stop times (on the order of 3 ms).

In extreme military environments, limited environmental control is
desirable for present magnetic tapes both during shipment and while
in operation.   Although it is possible to use magnetic tapes at temp-
erature and humidity extremes, the desirable operative range for
magnetic tapes is 65-85°F. with 40-60% relative humidity.   Storage
requirements are normally 40-90°F. with 20-80% relative humidity.
Most tapes will melt or burn, and stored data will be lost completely

if the tape is heated beyond the Curie point of the magnetic material. Shock or exposure to electrical, nuclear, or magnetic environments can also cause loss of data. The tape itself can be damaged by many chemical atmospheres and solvents. However, the Achilles heel of a militarized magnetic tape system is not the magnetic tape but the tape transport.

All present tape transports require the physical movement of a very thin (approximately 1 mil) piece of oxide coated tape at high speeds (100-200 inches per second) across a highly sensitive read/write head. The iron oxide acts as an abrasive; therefore head wear and tape wear are inevitable. Head wear produces a widening of the read/write gap with a resultant decrease in frequency response of the head. Tape wear produces dust particles that can cause errors unless constant cleaning is provided to remove the dust.

Good magnetic tape system performance is the result of three factors; fast start times, high tape speed, and small head gap sizes. These are the very items that produce wear and require frequent maintenance. High performance in conventional magnetic tape transports therefore require high maintenance.

Specifications for the Sylvania MT451 transport developed under Navy Contract NObsr87543 call for MTBF of 400 hours with 90% confidence. [15] They further require 15 minutes per day of scheduled maintenance plus 6 hours of scheduled maintenance every 30 days. The deficiencies of even this ruggedized magnetic tape unit are evident when it is realized that these units are intended to be used with computers such as the CP667 or the CP642 that provide MTBF in excess of 1800 hours with little scheduled maintenance required. The high maintenance requirements and low MTBF of magnetic tape units are a result of the

electromechanical strains that must be placed on the system in order
to achieve reasonable start-stop times and transfer rates. It is not
possible to eliminate those strains in a conventional magnetic tape
transport design without seriously degrading the performance of the
system. Effective use of the transport requires stopping and starting
the tape in a few milliseconds. In the case of the Sylvania transport,
tape is accelerated from a rest position to 100 inches per second in 3
milliseconds. This represents a total travel of the tape of 0.125 inches
during its acceleration period.

Considering the large amounts of wear and stress that are placed on
a magnetic tape, the reliability of current tape units is remarkable.
However, when they must be depended upon in a real time combat
situation, their performance, maintenance requirements, and MTBF
are major problems.

Both high maintenance requirements and low MTBF could be overcome
by developing a solid-state auxiliary storage unit as a magnetic tape
replacement. One approach is to provide a large on-line auxiliary
mass storage system "partitioned" so that sections or "reels" or blocks
are allocated to different computers or problems as required. However,
to effectively replace magnetic tape units in many applications (particu-
larly from a cost standpoint) it will be necessary to develop removable
storage modules that can be transported and plugged into a set of read-
write and control electronics much as a reel of tape is placed on a tape
transport.

On-line solid state auxiliary mass storage units capable of fulfilling
many of the requirements of a magnetic tape replacement are available
today (e.g. magnetic core mass memories); however, they are expensive
and are not removable for transportation or storage. Memory

technologies suitable for the development of this removable type of
memory must provide large capacity storage at a low cost per bit
including electronics, must be non-volatile, and must require little
or no power in the quiescent state. Compactness of storage is also
important since large amounts of such storage may be necessary.
The BORAM devices being developed under the sponsorship of the
USAER&DL at Ft. Monmouth offer a promise for providing these
characteristics in the future. [8]

Detailed investigation of mass storage techniques discussed in Appen-
dix B of this report cover several technologies that may be available
by 1970 for solid state mass storage.

For intermediate applications and applications where rotating equipment
can be tolerated, large fixed head disc or drum systems can be used.

In applications where the solid-state replacement for magnetic tape
is to function only as a program store, read-only memories such as
photographic storage may also be considered.

The portable and off-line storage concept of solid-state magnetic tape
replacement requires a storage media that is compact (in blocks of
several million characters), is easily and economically separable
from its electronics, has a very low cost per bit for the media with-
out electronics and controls, and can be packaged in a portable form
that is relatively insensitive to shipping and environmental damage.

Appendix B of this report indicates that BORAM type devices are the
best candidates since they can be more easily separated from drive
and control electronics at low cost. However, removable media random
access memories are also being developed (e. g. a removable core stack).

Removable disc storage systems offer an alternative as an intermediate
step between the all-solid-state replacement for magnetic tape units
and the present magnetic tape systems.

The functional replacement of magnetic tape transports with a "solid-
state" unit could offer many desirable features for military applications.
Among these are:

       Reduction in maintenance requirements.

       Substantial improvements in MTBF.

       Improved performance characteristics.

The greatest obstacle in the application of solid-state techniques to a
magnetic tape replacement will be their relatively high cost per bit of
storage.

4 SYSTEM ORGANIZATION TO MINIMIZE INPUT/OUTPUT

In large systems the greatest improvement in the performance of input/
output equipment can be achieved by avoiding input/output operations
wherever possible. By keeping the data within the system when it will
be required for reuse and by capturing data at the source, the need for
conventional input/output equipment can be reduced. For example, the
need for large printed reports can be reduced or eliminated when the
user is operating on line with the processor through a display console.
When the entire data base within the system is available to the user upon
request, he will have little need for reports and other off-line references
which may be out of date by the time they are used. The display con-
soles in present NTDS systems provide a good example of this approach
with input and output being handled directly on-line through the user
consoles. The major use of conventional types of input/output equip-
ment in NTDS has been reduced to that of loading and changing of
programs.

Hardware developments such as the availability of low cost solid-state on-line auxiliary storage are essential to the implementation of this approach, but otherwise the solution is primarily a matter of systems design. Hence, this approach to solving the problem of imbalance between input/output equipment and central processor can only be recommended here. The development of this approach is outside the scope of this study but should be considered in related systems design studies. To achieve the improvements possible in this area will require a combined effort of users, programmers, hardware engineers, and systems planners and designers.

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Appendix E

INFORMATION SOURCES

1 ORGANIZATIONS CONTACTED

Advanced hardware technologies and applications in tactical military
systems have been discussed during visits with personnel in a
number of different companies, universities, and governmental
agencies in the course of this study. Informal discussions of
hardware technologies have also been held with many other people
in other organizations in telephone conversations or personal
discussions during conferences. Much appreciation is due these
people for their help and advice. In addition to the organizations
listed here, some of the information in this study was also obtained
in previous visits with other companies and organizations during
the ANTACCS Study in 1964. Those companies and organizations
are listed in the ANTACCS Final Report.

<u>Commercial and Non-Profit Organizations:</u>

Ampex	Culver City, California
Autonetics	Anaheim, California
Bunker Ramo Corporation	Canoga Park, California
Burroughs Corporation	Paoli, Pennsylvania
Burroughs Corporation	Pasadena, California
Corning Glass Works	Raleigh, North Carolina
Digidata Corporation	Washington, D.C.
Fairchild Semiconductor Division	Palo Alto, California
Farrington Corporation	Washington, D.C.
General Dynamics Electronics	San Diego, California
General Electric TEMPO	Washington, D.C.
General Electric	Syracuse, New York

General Kinetics	Washington, D. C.
Hamilton Standard Division, United Aircraft	Broadbrook, Connecticut
Honeywell	Wellesley Hills, Massachusetts
IBM Research Laboratory	Yorktown Heights, New York
Informatics Inc.	Los Angeles, California
Kennedy Corporation	Pasadena, California
Laboratory for Electronics	Boston, Massachusetts
Librascope Group General Precision Inc.	Los Angeles, California
Litton Industries	Los Angeles, California
MIT Project MAC	Boston, Massachusetts
Norden Division United Aircraft	Norwalk, Connecticut
Philco Corporation	Philadelphia, Pennsylvania
Potter Instruments Company	Plainview, New York
RAND Corporation	Santa Monica, California
Recognition Equipment Co.	Dallas, Texas
Stanford Research Institute	Menlo Park, California
Stanford University	Palo Alto, California
Sylvania Corporation	Needham, Massachusetts
Teledyne Inc.	Hawthorne, California
Univac Division Sperry Rand Corporation	Blue Bell, Pennsylvania
Westinghouse Molecular Electronics Division	Baltimore, Maryland
Xerox Corporation	Rochester, New York

Government and Military Agencies

Department of Defense, DDR&E	Washington D. C.
NASA Headquarters	Washington D. C.
Naval Air Development Center	Johnsville, Pennsylvania
Naval Applied Science Laboratory	Brooklyn, New York
Naval Aviation Facility (NAFI)	Indianapolis, Indiana
Naval Electronics Laboratory	San Diego, California
Naval Ordnance Test Station	China Lake, California
Naval Research Laboratory	Washington, D. C.
Office of Naval Research	Washington, D. C.
ONR Communication Study Group	Washington, D. C.
Rome Air Development Center	Rome, New York
U.S. Army Automatic Field System Command	Fort Belvoir, Virginia
U.S. Army Engineering R&D Laboratory	Fort Monmouth, New Jersey
U.S. Marine Corps, Bureau of Ships	Washington, D. C.
U.S. Navy, Bureau of Ships	Washington, D. C.
U.S. Navy, OpNav	Washington, D. C.
U.S. Navy Shore Electronics Equipment Command	Washington, D. C.
USS Kitty Hawk	San Diego, California
Wright Air Development Center	Dayton, Ohio

Discussions with personnel of these organizations provided a basis for
much of the information presented in this report. In addition to discussing
techniques and approaches that have not been adequately described in pub-
lished literature, the opinions of experts in specific areas in these organi-
zations were solicited concerning the advantages, disadvantages, limitations
and future prospects for different technologies.

2 CONFERENCES, SYMPOSIA, AND MEETINGS

During this study, a number of conferences, symposia, and technical
meetings were attended. Attendance at these meetings provided valuable infor-
mation   for this study of hardware technology not only through the
formal papers presented at the meetings but also through the
opportunity to participate in discussions and panels, to view the
hardware exhibits, and to engage in informal personal discussions
with specialists and experts in each area of technology covered by
the study. The conferences, symposia and meetings attended during
the study are listed below.

IEEE Computer Group Symposium on the Impact of Batch Fabrication
on Future Computers, Los Angeles, California

IEEE Computer Group Workshop on Impact of Large Scale Integration
on Information Processing Systems, Lake Arrowhead, California

IEEE Computer Group Workshop on Batch Fabricated Memory
Technologies, San Francisco, California

IEEE Computer Group Display Devices Workshop, San Francisco, California

1965 IFIPS Conference, New York, New York

Orange County IEEE Computer Group Meeting on Optical Data
Processing, Orange County, California

Orange County IEEE Computer Group Meeting on New Hardware
Developments in Information Display, Orange County, California

Orange County IEEE Computer Group Panel Discussion on Aerospace
Computers, Orange County, California

SDC/ARPA/ESD Conference, Second Symposium on Computer
Centered Data Base Systems, Santa Monica, California

Second Conference on Digital and Hybrid Shipboard Control Systems,
U. S. NOTS, China Lake, California

Society for Information Display Seminar on Summary of New Ideas
and New Directions in Displays, Santa Monica, California

Society for Information Display, 5th National Symposium on
Information Display, Santa Monica, California

Society for Information Display, 6th National Symposium on
Information Display, New York, New York

1965 Fall Joint Computer Conference, Las Vegas, Nevada

1966 Spring Joint Computer Conference, Boston, Massachusetts

1966 Fall Joint Computer Conference, San Francisco, California

1965 WESCON, San Francisco, California

1966 WESCON, Los Angeles, California

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In addition to the specific references listed in each appendix covering
the four major areas of technology, information from many other
published sources were used as a basis for the data, analyses, and
conclusions presented in this report.   These published sources
included descriptive brochures and reports on commercial developments,
technical reports on government sponsored development programs,
reports on Navy and Marine Corps applications and systems,
proceedings of technical conferences and symposia, books on
hardware technologies, and many technical magazine articles.   These
reports, books, proceedings, and magazines are identified in the
following bibliography.

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Computer Design

Control Engineering

Datamation

Data Systems Design

Electrical Design News

Electromechanical Design

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Electronics

Electro-Technology

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13 ABSTRACT

This report presents results of an analysis and evaluation of trends in the
application of advanced data processing technology for future Naval
tactical data systems. This study, sponsored by the Office of Naval
Research and Ships Systems Command, covered a critical analysis and
evaluation of hardware technologies that will be feasible for use in 1970-
1980 era tactical military computers and data systems. This study in-
cluded an evaluation of research and development activities in the areas
of memories, component and packaging techniques, displays, and input/
output equipment. It emphasized the effect of new technologies on the
design and operation of future systems and the requirements placed on
hardware technology by future trends in computer systems design.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Computers						
Data Processing System						
Command & Control System						
Displays						
Storage						
Memories						
Logic Components						
Integrated Circuits						
Input/Output Equipment						
Packaging						
Maintainability						

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